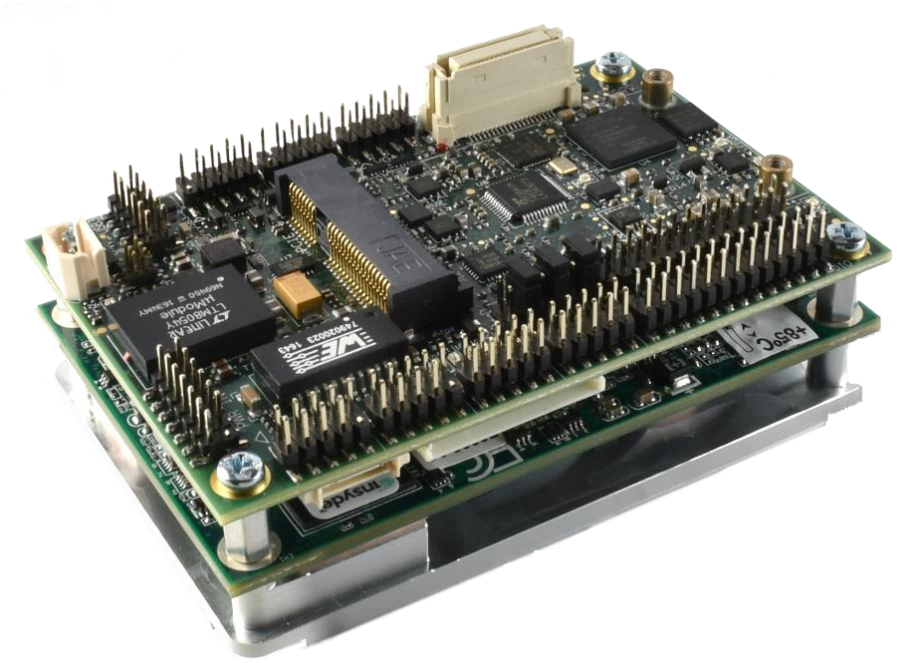


ZETA

COM-based SBC based on

Type 10 nano COM Modules

Revision	Date	Comment
1.0	9/6/2018	Initial release from v0.7

FOR TECHNICAL SUPPORT
PLEASE CONTACT:

support@diamondsystems.com

CONTENTS

1 Important Safe Handling Information

WARNING!

ESD-Sensitive Electronic Equipment

Observe ESD-safe handling procedures when working with this product.
Always use this product in a properly grounded work area and wear appropriate ESD-preventive clothing and/or accessories.
Always store this product in ESD-protective packaging when not in use.

Safe Handling Precautions

The Zeta baseboard contains a high number of I/O connectors with connection to sensitive electronic components. This creates many opportunities for accidental damage during handling, installation and connection to other equipment. The list here describes common causes of failure found on boards returned to Diamond Systems for repair. This information is provided as a source of advice to help you prevent damaging your Diamond (or any vendor's) embedded computer boards.

ESD damage – This type of damage is usually almost impossible to detect, because there is no visual sign of failure or damage. The symptom is that the board eventually simply stops working, because some component becomes defective. Usually the failure can be identified and the chip can be replaced.

To prevent ESD damage, always follow proper ESD-prevention practices when handling computer boards.

Damage during handling or storage – On some boards we have noticed physical damage from mishandling. A common observation is that a screwdriver slipped while installing the board, causing a gouge in the PCB surface and cutting signal traces or damaging components.

Another common observation is damaged board corners, indicating the board was dropped. This may or may not cause damage to the circuitry, depending on what is near the corner. Most of our boards are designed with at least 25 mils clearance between the board edge and any component pad, and ground / power planes are at least 20 mils from the edge to avoid possible shorting from this type of damage. However, these design rules are not sufficient to prevent damage in all situations.

A third cause of failure is when a metal screwdriver tip slips, or a screw drops onto the board while it is powered on, causing a short between a power pin and a signal pin on a component. This can cause overvoltage / power supply problems described below. To avoid this type of failure, only perform assembly operations when the system is powered off.

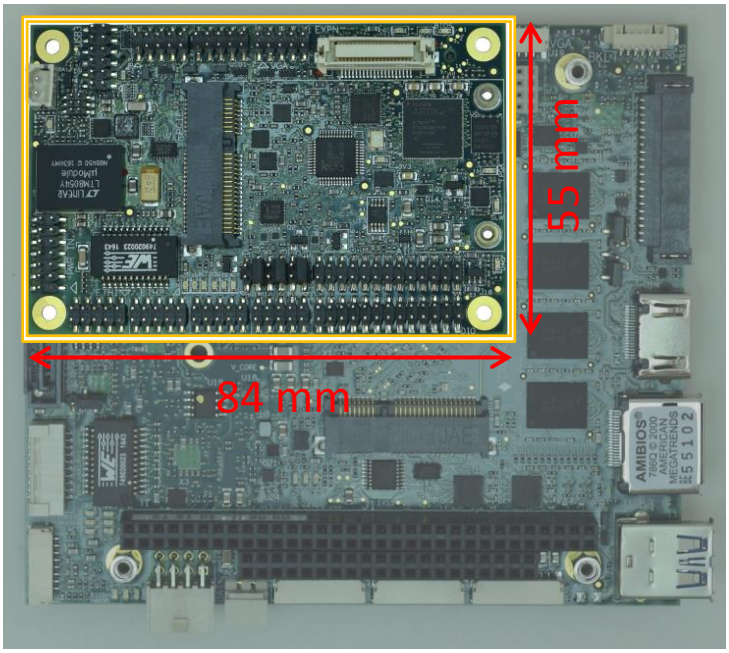
Sometimes boards are stored in racks with slots that grip the edge of the board. This is a common practice for board manufacturers. However, our boards are generally very dense, and if the board has components very close to the board edge, they can be damaged or even knocked off the board when the board tilts back in the rack. Diamond recommends that all our boards be stored only in individual ESD-safe packaging. If multiple boards are stored together, they should be contained in bins with dividers between boards. Do not pile boards on top of each other or cram too many boards into a small location. This can cause damage to connector pins or fragile components.

Power supply wired backwards – Our power supplies and boards are not designed to withstand a reverse power supply connection. This will destroy each IC that is connected to the power supply (i.e. almost all ICs). In this case the board will most likely will be unrepairable and must be replaced. A chip destroyed by reverse power or by excessive power will often have a visible hole on the top or show some deformation on the top surface due to vaporization inside the package. **Check twice before applying power!**

Bent connector pins – This type of problem is often only a cosmetic issue and is easily fixed by bending the pins back to their proper shape one at a time with needle-nose pliers. The most common cause of bent connector pins is when a PC/104 board is pulled off the stack by rocking it back and forth left to right, from one end of the connector to the other. As the board is rocked back and forth it pulls out suddenly, and the pins at the end get bent significantly. The same situation can occur when pulling a ribbon cable off of a pin header. If the pins are bent too severely, bending them back can cause them to weaken unacceptably or even break, and the connector must be replaced.

2 Introduction

Zeta is a miniature embedded computer consisting of two boards: a COM (computer on module), which provides the CPU and related core functionality, and a baseboard, which provides the "final inch" of I/O such as Ethernet magnetics, serial port transceivers, power supply, and real-world I/O. Zeta is based on the COM Express "type 10" or "mini" form factor, which is one of the smallest industry-standard COM form factors for x86 processors, measuring only 55 x 84 mm / 2.2 x 3.3 inches. The use of a miniature COM plus a same-size baseboard enables Zeta to deliver an impressive array of features and performance in a very small size, achieving as much as a 60% reduction in area compared to other form factors such as PC/104.



The Zeta SBC offers equivalent performance to Diamond's Aries SBC at only 40% the size.

2.1 Available Configurations

Zeta is available in two major configurations: DAQ (full data acquisition, model numbers ending in A) and DIO (digital I/O only, model numbers ending in D). Each configuration is offered with 3 choices of COMs, offering 3 different options of processor / performance / memory / price.

Model	ZETA-E3815-2GA/D	ZETA-E3940-4GA/D	ZETA-N4200-8GA/D
Processor	Intel "Bay Trail" E3815	Intel "Apollo Lake" E3940	Intel "Apollo Lake" N4200
CPU clock rate	1.33GHz dual core	1.6GHz quad core	1.1GHz quad core
Passmark rating			
Memory	2GB DDR3L	4GB DDR3L	8GB DDR3L
LCD	Single-channel 24-bit up to 1920 x 1200		
Power consumption			

Core I/O features common to all models of Zeta include the following:

Feature	Value
Serial ports	4x RS-232/422/485
USB2.0	4
USB3.0	1
Input voltage	6-36VDC
Gigabit Ethernet ports	2
VGA display	1
LVDS display	1 single channel
Micro-SD socket	1
Mini PCIe / mSATA socket	1
Expansion connector	PCIe x 1 – 2 ports SATA – 1 port HD audio - 1 I2C – 1 channel USB 2.0 – 1 port

Data acquisition / digital I/O features are as follows:

Feature	A model with DAQ	D model with DIO
Analog inputs	16 single-ended / 8 differential, 16-bit resolution, 100KHz max sample rate	-
Input ranges	0-10V, 0-5V, +/-10V, +/-5V	-
Analog outputs	4 16-bit	-
Output ranges	0-5V, 0-2.5V	-
Digital I/O	27 lines organized as 2 8-bit ports and 11 1-bit ports	16 lines organized as 2 8-bit ports
DIO features	Each port programmable in/out; all ports configurable for 3.3V or 5V logic compatibility and pull-up/pull-down resistors	Each port programmable in/out; all ports configurable for 3.3V or 5V logic compatibility and pull-up/pull-down resistors
Counter/timers	8 32-bit counters with up/down counting and internal/external clock selection; programmable interrupt capability	-
PWM	4 24-bit PWMs with 0-100% duty cycle programmability	-

2.2 Mechanical, Electrical, Environmental

- Dimensions 55 x 84 mm / 2.16” x 3.30”
- Cooling Conduction Cooling via heat spreader mounted on the bottom
- Power input 6V to +36V standard; fixed 12V optional with minimum order quantity
- Operating Temp -40°C to +85°C at the external surface of the heat spreader

2.3 Operating System Support

- Linux Ubuntu 16.04 LTS (all models)
- Windows 7 (E3815 models only)
- Windows 10 IoT (E3940 / N4200 models only)

3 Block Diagram

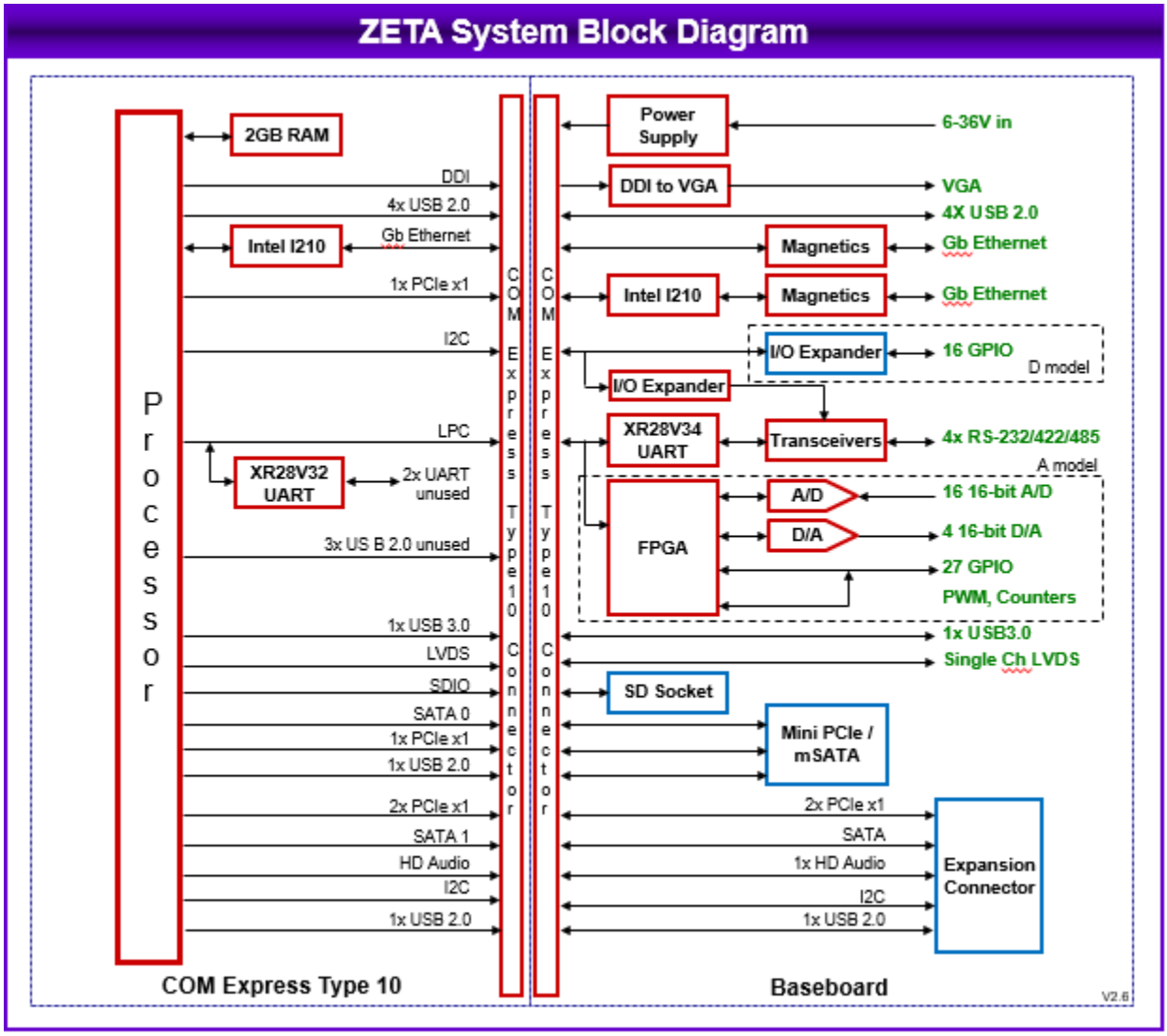


Figure 1: Functional Block Diagram

4 Feature Description

4.1 Power Supply

Zeta base board can be powered either from any DC power supply with an output voltage range of +6V to +36V. This range makes Zeta compatible with standard power supply voltages of 12V, 24V, and 28V. In addition, Zeta can operate in a vehicle environment due to its ability to run on 6VDC.

Maximum allowable reflected ripple, measured at the voltage input connector is 50mV p-p.

4.2 Ethernet

Zeta base board supports one standard and one optional 10/100/1000 Ethernet port. The standard port comes directly from the COM module. The optional port is derived from the Intel WGI210IT PCIe Ethernet controller. This controller is accessed via x1 PCIe lane from the COM. Both ports have on-board magnetics to allow use with a DSC standard Ethernet cable.
On-board LEDs are provided for Link, Activity, and Speed on each port. The LEDs are located along the board edge near the Ethernet connectors. Both connectors provide access to the LED signals.

4.3 Micro SD

Zeta base board supports one micro SD connector with 4-bit data 3.3V for an additional low-cost storage option.

4.4 USB

Zeta base board supports 6 USB2.0 ports and one USB 3.0 port.

- Four USB2.0 ports are routed to 2x5 headers for use with cables.
- One USB2.0 port is interfaced to the PCIe Mini card socket to support USB minicards.
- One USB2.0 port is routed to Expansion connector for use on installed daughterboards.
- The USB 3.0 port is routed to a 2x6 pin header. This pin header is compatible with the Intel standard dual USB 3.0 connector for convenience.

4.5 VGA

Zeta base board supports VGA display interface. DDI to VGA converter chip (CH7517) is used to covert DDI from COM connector to VGA signals.

4.6 LCD

Zeta supports a 24-bit single channel LVDS display through a 1x20 RA latching connector. Separate backlight supply connector provides LCD backlight supply and PWM control. Backlight supply is given externally through the main power input connector.

4.7 Audio

HD audio from the COM is available on the expansion connector. A daughterboard is required to utilized the audio feature.

4.8 Serial Ports

Zeta supports 4 serial ports using an LPC UART (XR28V384). UARTs from the COM are not utilized. Protocol selection and RS-422/485 line termination are provided using an I2C digital I/O expander chip driven by the COM. The configuration can be done in the BIOS and also via user application software.

4.9 RTC Backup Battery

A 2x1 connector is provided for connecting an external backup battery to maintain the real-time clock. The allowable battery voltage range is 3.0 – 3.6VDC.
The backup battery is not required to maintain custom BIOS settings.

4.10 mSATA/PCIe Mini-card Socket

Zeta provies one mSATA/Mini PCIe socket. This socket supports full-size PCIe Minicards and mSATA cards.

4.11 PCIe Link Routing

Zeta base board makes use of 3 PCIe lanes from the COM connector

- Lane 1 – MiniPCIe socket
- Lane 2 – Second Gigabit Ethernet through i210 Ethernet controller
- Lane 3 – EMX expansion socket
- Lane 4 – EMX expansion socket (Not available in EmNANO i2300)

4.12 Data Acquisition

Zeta base board provides a data acquisition sub circuit containing analog input, analog output, and digital I/O features. This circuit is controlled by an FPGA attached to the processor via the LPC bus. A pin header on the board provides access to JTAG signals for reprogramming the FPGA on the board and in the field.
The data acquisition circuit is based on the Diamond Zeta base board.
Features include:
16 single-ended / 8 differential analog inputs with 16-bit resolution, programmable input ranges, and 100KHz sample rate;
4 analog outputs with 16-bit resolution and programmable output ranges
27 digital I/O lines with selectable 3.3V/5V logic levels, selectable pull-up/down resistors, programmable direction, buffered I/O, and capability for use as counter/timer and PWM circuits.

4.13 GPIO

16 GPIO are available via I2C expander circuit (PCA9535) on the digital I/O header for Low cost version, when Data acquisition circuit is not populated.

4.14 LED Indicators

Zeta provides the following LED indicators.

- Power on -Green LED (for 12V, 5V and 3.3V)
- Power Good -Green LED for Power Good indication
- BIOS LED -Green LED to indicate Module is booted successfully
- Ethernet -Green LED for Link, activity, and speed for each port

4.15 Expansion Connector

Zeta supports I/O expansion capability using a high-density 40-pin expansion connector. A daughterboard is available from Diamond Systems utilizing the expansion signals to provide additional I/O and mass storage capability. Users can also design their own custom I/O daughterboards to provide custom I/O.

- Two PCIe x 1 lanes
- HD Audio interface
- SATA interface
- USB2.0 interface
- I2C interface

5 Mechanical Drawing

The form factor of the board is COM Express Nano Type 10 with dimensions 55mm x 84mm.

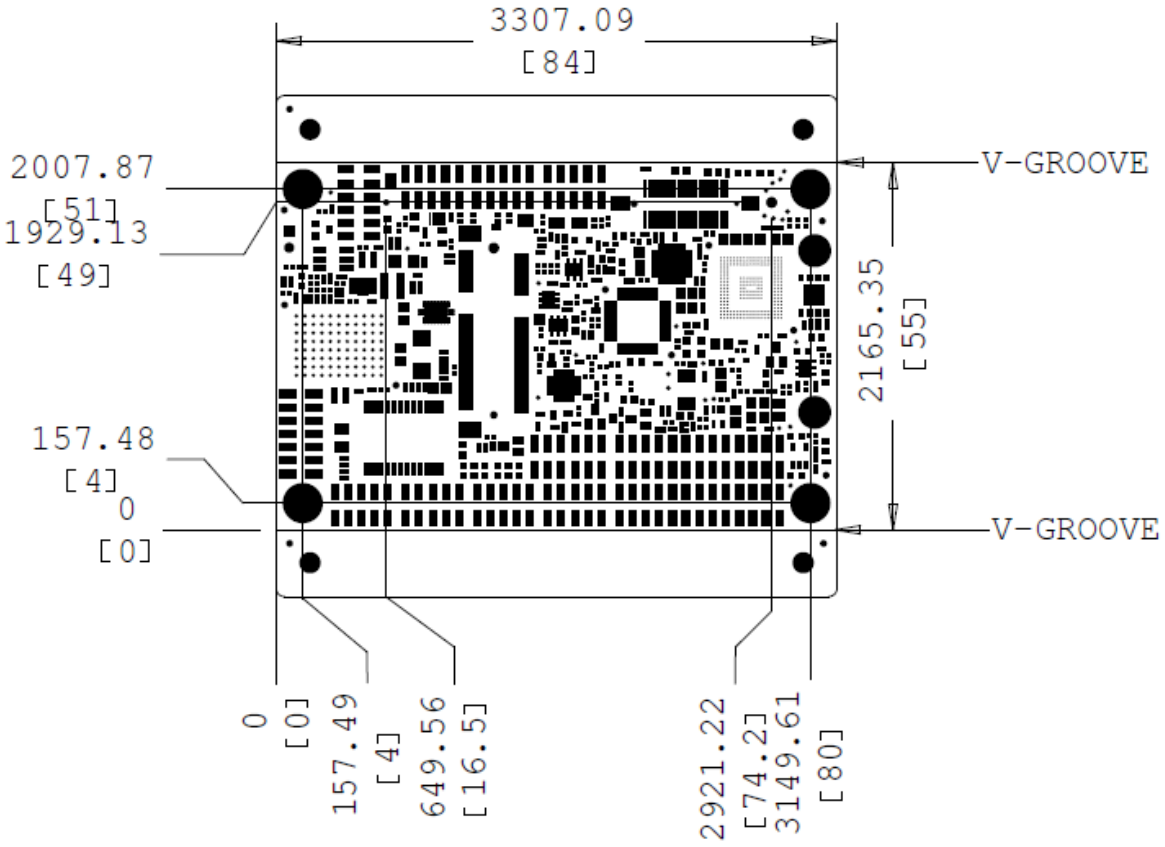


Figure 2: Mechanical outline, top view

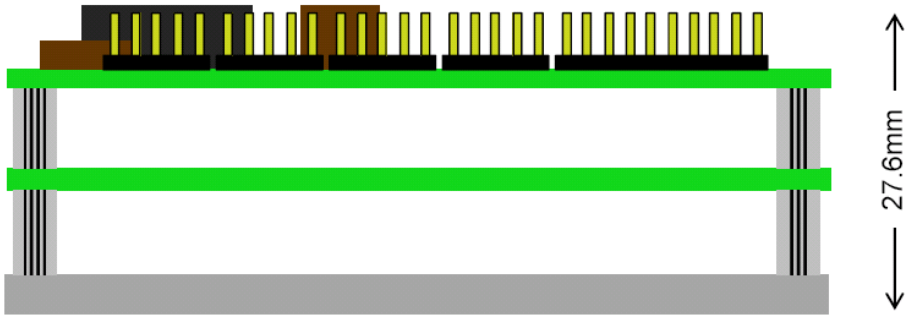


Figure 3: Mechanical outline, Side view

6 I/O Connector and Jumper Locations

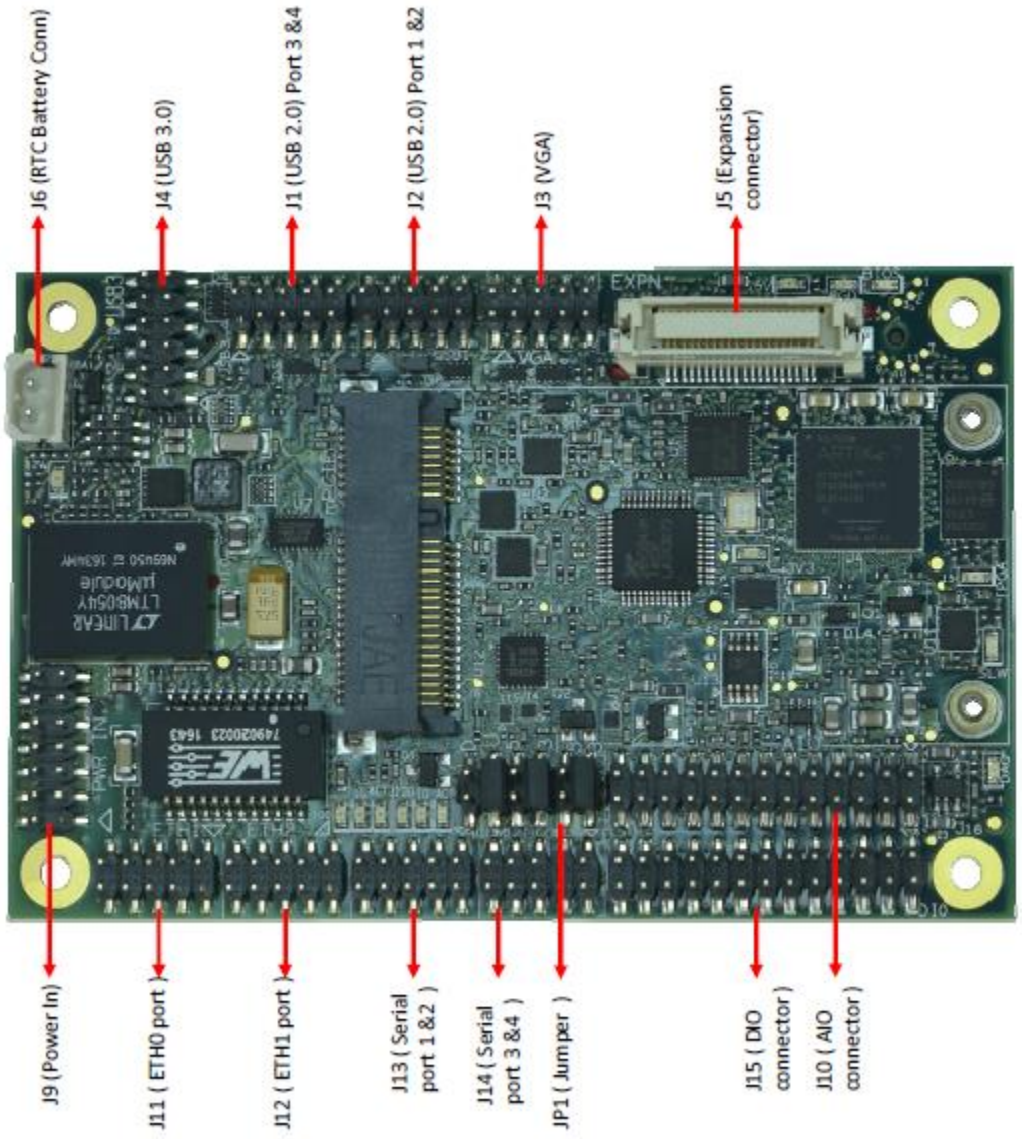


Figure 4 : Zeta board connectors and jumpers - Top side

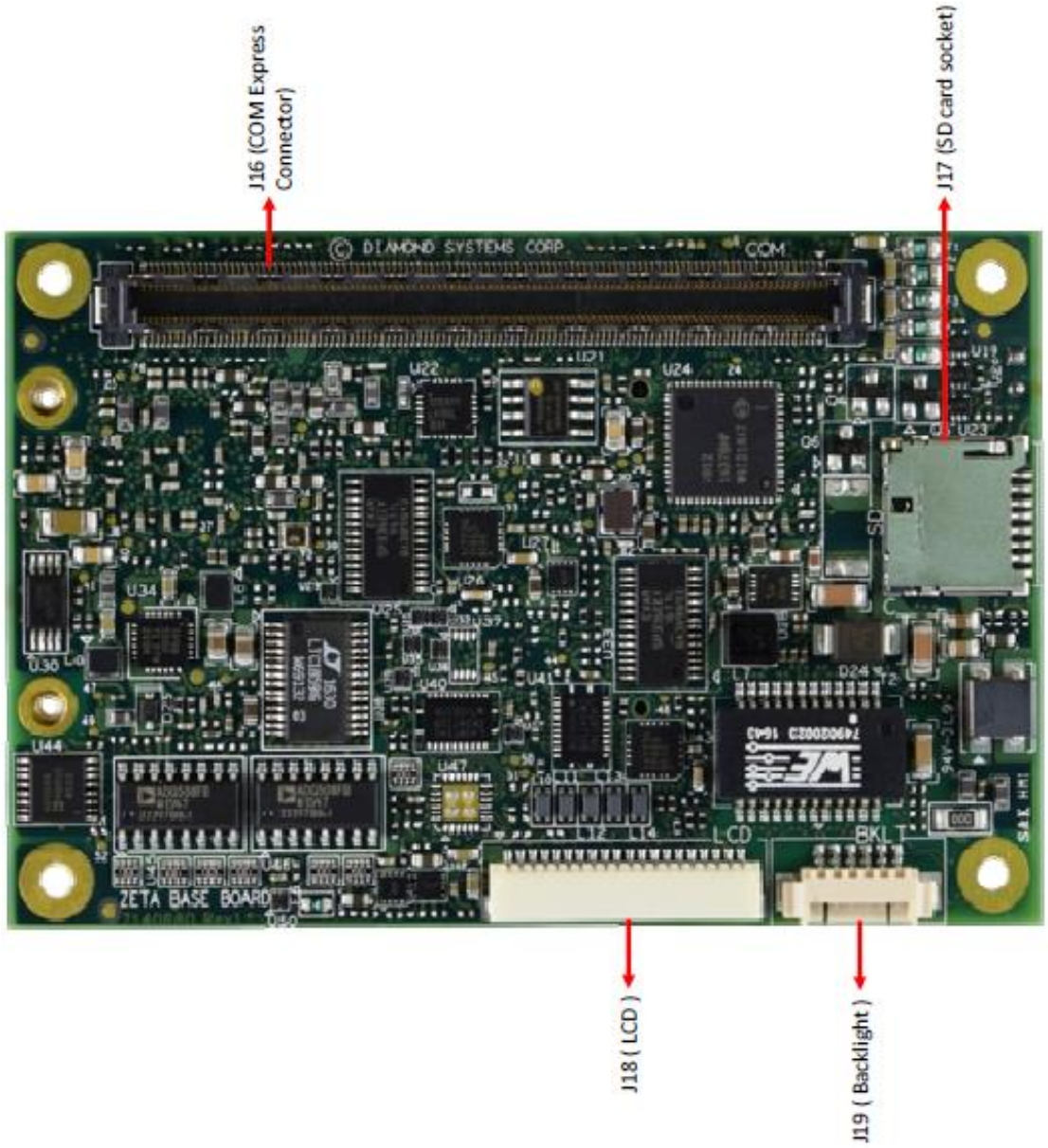


Figure 5 : Zeta board connectors - Bottom side

7 Getting started

7.1 Development Kit

Zeta is available in a complete development kit that includes a full set of I/O cables and the selected SDK. Simply install the pre-configured flash disk, attach cables / keyboard / mouse / monitor, power up, and the system is ready to run.

7.2 Development Kit Contents

- Zeta SBC with DAQ
- Zeta Cable Kit CK-ZETA-01
- 32GB MLC mSATA flash-disk with bootable image
- Zeta Development kit user manual

7.3 System Setup

1. Attach the VGA cable 6981084 and USB cables 6981082 as needed.
2. Attach display, keyboard, and mouse (if needed) to the cables.
3. Check the jumpers as described in Section 7 for a default settings or change as desired.
4. Connect power to power input connector J9 using your own power supply with power cable 6981070. The input connector and cable are keyed to prevent incorrect connection.
   WARNING: Attaching the power connector incorrectly will destroy the Zeta base board!

For a quick verification that the system is set up and working properly, if no boot device is attached, the system will boot to shell utility in case of Arbor module.

7.4 Boot Device Options

Zeta base board can boot from mSATA or any of the available USB ports or micro SD card (linux only). Diamond Systems' software and hardware development kits include a mSATA with pre-loaded OS.
Zeta base board can be booted from micro SD card for linux OS. Zeta base board can be booted from an external hard drive connected mini card to SATA adapter board.

WARNING: It is possible to destroy the Helix SBC by connecting a SATA cable incorrectly (reverse orientation or offset from correct position). Always use keyed cables to avoid connection errors.

The Boot device selection and priority are configured in the BIOS **Boot** menu. Only devices which are connected to the SBC will appear in the list of options. Therefore, if user wants to select a hard drive or USB device as the boot device, the SBC should be connected first, then boot up, enter the BIOS, and select the desired device as the boot device. Boot type order can be changed using '+'/'-' key.

The following are a few examples of boot scenarios.

- Attach a mSATA device on the shared mSATA / PCIe MiniCard socket
- Attach a bootable USB device to one of the USB ports
- Attach a M.2 SATA SSD to M.2 socket on daughter board

- Connect an externally powered SATA hard drive to shared mSATA / PCIe MiniCard socket using mini card to SATA adapter board
- PXE boot
- Micro SD Card (linux only)

7.5 Installing OS and Booting

The following steps describe how to install an operating system from a mSATA using Arbor module. Follow the below steps to install a 32-bit Windows 7 legacy operating system on a mSATA.

- Connect a USB pen drive to a USB port of (J1 or J4) of Zeta base board having 32-bit Windows 7 installation image.
- Power ON the board.
- Enter the BIOS menu by pressing DEL key. The mSATA and USB device should be detected in BIOS under boot devices.
- Under Boot Type Order, set the highest priority for USB.
- Save the BIOS settings and restart.
- The Windows 7 installer will start running. Follow the instructions to complete the installation.
- Upon successful installation, boot to Windows 7 and install the necessary drivers.
- Upon restart, to boot from mSATA, go to BIOS menu and under Boot Type Order set highest priority to Hard disk.

8 Connector Pinout and Signal Description

8.1 Power Input (J9)

The pinout of the power input connector is shown below. Although 4 power and 6 ground pins are provided, not all pins need to be connected. Each connector pin can support up to 2A. The number of connections can be determined by the total power consumption of the Zeta board plus all attached I/O (daughterboard, mSATA and mini PCIe modules, and USB devices) divided by the input voltage, divided by 2A.

Key	1	2	GND
VIN	3	4	GND
VIN	5	6	GND
VIN	7	8	GND
VIN	9	10	GND
SYS_RST_R#	11	12	GND
VCC_5V/12P0_BKLT	13	14	PWRBTN#

8.2 RTC Battery input (J6)

The pinout for the RTC battery connector is shown below. The battery input voltage range is 3.0 – 3.6VDC.

RTC_BATT	1
GND	2

8.3 Serial Ports (J13 and J14)

Serial ports 1 and 2 are provided on connector J13, and serial ports 3 and 4 are provided on connector J14.All four serial ports support RS422, RS422 and RS485 modes.

8.3.1 RS232 mode

TX1	1	2	RTS1
RX1	3	4	CTS1
GND	5	6	GND
TX2	7	8	RTS2
RX2	9	10	CTS2

TX3	1	2	RTS3
RX3	3	4	CTS3
GND	5	6	GND
TX4	7	8	RTS4
RX4	9	10	CTS4

8.3.2 RS422 mode

TX1+	1	2	TX1-
RX1+	3	4	RX1-
GND	5	6	GND
TX2+	7	8	TX2-
RX2+	9	10	RX2-

TX3+	1	2	TX3-
RX3+	3	4	RX3-
GND	5	6	GND
TX4+	7	8	TX4-
RX4+	9	10	RX4-

8.3.3 RS485 mode

TX1/RX1+	1	2	TX1/RX1-
NC	3	4	NC
GND	5	6	GND
TX2/RX2+	7	8	TX2/RX2-
NC	9	10	NC

TX3/RX3+	1	2	TX3/RX3-
NC	3	4	NC
GND	5	6	GND
TX4/RX4+	7	8	TX4/RX4-
NC	9	10	NC

8.4 USB 2.0 Ports (J2 and J1)

USB port 0 and 1 are provided on connector J2, and USB port 2 and 3 are provided on connector J1. Pinout for the connector is shown below:

Key	1	2	Shield
GND (USB1 Pwr-)	3	4	GND (USB0 Pwr-)
USB1 Data+	5	6	USB0 Data+
USB1 Data-	7	8	USB0 Data-
USB1 Pwr+	9	10	USB0 Pwr+

Key	1	2	Shield
GND (USB3 Pwr-)	3	4	GND (USB2 Pwr-)
USB3 Data+	5	6	USB2 Data+
USB3 Data-	7	8	USB2 Data-
USB3 Pwr+	9	10	USB2 Pwr+

8.5 USB 3.0 Port (J4)

One USB 3.0 port is provided on connector J4. The pinout for the connector is shown below:

USB Pwr+	1	2	NC
USB_SSRX0-	3	4	USB Pwr+
USB_SSRX0+	5	6	NC
GND (USB Pwr-)	7	8	NC
USB_SSTX0-	9	10	GND (USB Pwr-)
USB_SSTX0+	11	12	NC

8.6 Ethernet (J11 and J12)

Two 10/100/1000 BASE-T Ethernet ports are provided on connectors J11 and J12. The connector pinouts are shown below. Port 1 is derived from the COM, and port 2 is derived from an Intel i210 PCIe Ethernet controller on the baseboard.

NC	1	2	CH1_Key
CH1_D0+	3	4	CH1_D0-
CH1_D1+	5	6	CH1_D1-
CH1_D2+	7	8	CH1_D2-
CH1_D3+	9	10	CH1_D3-

NC	1	2	CH2_Key
CH2_D0+	3	4	CH2_D0-
CH2_D1+	5	6	CH2_D1-
CH2_D2+	7	8	CH2_D2-
CH2_D3+	9	10	CH2_D3-

8.7 mSATA / mPCIe (J8)

mSATA and mPICe cards are supported on connector J8. All TX/RX signals are with respect to the host. TX on the socket drives RX on the installed module, and RX on the socket is driven by TX on the installed module. The pinout for the connector is shown below. The two mounting standoffs at the far end of the module installation site are not connected to ground.

PCIe MiniCard	mSATA			mSATA / PCIe MiniCard
Wake-		1	2	+3.3V
NC	NC	3	4	Gnd
NC	NC	5	6	+1.5V
Clkreq-		7	8	NC
Gnd	Gnd	9	10	NC
PCIe 0 Clk-	PCIe 0 Clk- *	11	12	NC
PCIe 0 Clk+	PCIe 0 Clk+ *	13	14	NC
Gnd	Gnd	15	16	NC
		KEY		
NC	NC	17	18	Gnd
NC	NC	19	20	Disable-
Gnd	Gnd	21	22	PCIe Reset-
PCIe 0 RX-	**SATA 0 RX+**	23	24	+3.3V
PCIe 0 RX+	**SATA 0 RX-**	25	26	Gnd
Gnd	Gnd	27	28	+1.5V
Gnd	Gnd	29	30	SMB Clk
PCIe 0 TX-	**SATA 0 TX-**	31	32	SMB Data
PCIe 0 TX+	**SATA 0 TX+**	33	34	Gnd
Gnd	Gnd	35	36	USB2_N
Gnd	Gnd	37	38	USB2_P
+3.3V	+3.3V	39	40	Gnd
+3.3V	+3.3V	41	42	WWAN LED-
Ground	Ground	43	44	WLAN LED-
NC	NC	45	46	WPAN LED-
NC	NC	47	48	+1.5V
Pull-up to +3.3V	Pull-up to +3.3V	49	50	Gnd
NC	NC	51	52	+3.3V
GND	GND	P1	P2	GND

8.8 Micro SD (J17)

A Micro SD card is supported on connector J17.The Micro SD can be used as a boot device or storage device in Linux. It can be used only as a storage device in Windows 7 and 10.

1	DAT2
2	CD/DAT3
3	CMD
4	VDD 3.3V
5	CLK
6	Ground
7	DAT0
8	DAT1

8.9 VGA (J3)

The VGA interface is provided on connector J3. Pinout for the connector is shown below:

RED	1	2	Ground
GREEN	3	4	Key
BLUE	5	6	Ground
HSYNC	7	8	DDC-Data
VSYNC	9	10	DDC-Clock

8.10 LVDS (J18)

The single-channel LVDS interface is provided on connector J18. The pinout is shown below:

VCC_5V_LVDS_CON	1
V_3P3_LVDS_CON	2
LVDS_A_CH_CLK_P	3
LVDS_A_CH_CLK_N	4
GND	5
LVDS_A_CH_0_P	6
LVDS_A_CH_0_N	7
GND	8
LVDS_A_CH_1_P	9
LVDS_A_CH_1_N	10
GND	11
LVDS_A_CH_2_P	12
LVDS_A_CH_2_N	13
GND	14
LVDS_A_CH_3_P	15
LVDS_A_CH_3_N	16
LVDS_DDC_CLK	17
LVDS_DDC_DAT	18
GND	19
GND	20

8.11 LCD Backlight (J19)

The pinout for the connector is shown below:

1	Power +5V/+12V
2	Power +5V/+12V
3	Ground
4	Ground
5	LCD backlight Enable signal
6	LCD PWM signal

8.12 Analog I/O (J10)

The pinout for the connector is shown below:

Vout 0	1	2	Vout 1
Vout 2	3	4	Vout 3
Aground	5	6	Aground
Vin 0 / 0+	7	8	Vin 8 / 0-
Vin 1 / 1+	9	10	Vin 9 / 1-
Vin 2 / 2+	11	12	Vin 10 / 2-
Vin 3 / 3+	13	14	Vin 11 / 3-
Vin 4 / 4+	15	16	Vin 12 / 4-
Vin 5 / 5+	17	18	Vin 13 / 5-
Vin 6 / 6+	19	20	Vin 14 / 6-
Vin 7 / 7+	21	22	Vin 15 / 7-
DIO D0	23	24	DIO D1
DIO D2	25	26	Dground

Note: This connector will not be used in D-model.

8.13 Digital I/O (J15)

The pinout for the Zeta A model is shown below.

DIO A0	1	2	DIO A1
DIO A2	3	4	DIO A3
DIO A4	5	6	DIO A5
DIO A6	7	8	DIO A7
DIO B0	9	10	DIO B1
DIO B2	11	12	DIO B3
DIO B4	13	14	DIO B5
DIO B6	15	16	DIO B7
DIO C0	17	18	DIO C1
DIO C2	19	20	DIO C3
DIO C4	21	22	DIO C5
DIO C6	23	24	DIO C7
+5V/3.3V fused	25	26	Dground

The pinout for the Zeta D model is shown below.

DIO A0	1	2	DIO A1
DIO A2	3	4	DIO A3
DIO A4	5	6	DIO A5
DIO A6	7	8	DIO A7
DIO B0	9	10	DIO B1
DIO B2	11	12	DIO B3
DIO B4	13	14	DIO B5
DIO B6	15	16	DIO B7
NC	17	18	NC
NC	19	20	NC
NC	27	22	NC
NC	23	24	NC
+5V/3.3V fused	25	26	Dground

8.14 Expansion connector (J5)

The pinout for the connector is shown below. Pins with remark “(NC)” are not available with EmNANO i2300.

+5V	1	2	+5V
PCIe_Exp2_T+ (NC)	3	4	PCIe_Exp1_T+
PCIe_Exp2_T-(NC)	5	6	PCIe_Exp1_T-
Gnd	7	8	Gnd
PCIe_Exp2_R+(NC)	9	10	PCIe_Exp1_R+
PCIe_Exp2_R-(NC)	11	12	PCIe_Exp1_R-
Gnd	13	14	Gnd
PCIe_Exp2_C+(NC)	15	16	PCIe_Exp1_C+
PCIe_Exp2_C-(NC)	17	18	PCIe_Exp1_C-
+3.3V	19	20	Gnd
SATA-T+	21	22	PCIe_Exp1_clkreq-(NC)
SATA-T-	23	24	PCIe_Exp2_clkreq-(NC)
+3.3V	25	26	USB2_D4_P
SATA-R+	27	28	USB2_D4_N
SATA-R-	29	30	Gnd
+3.3V	31	32	Host Reset-
AC_SDIN0	33	34	I2C_Data
AC_BITCLK	35	36	I2C_Clk
AC_SDOUT	37	38	AC_SYNC
AC_RST#	39	40	Gnd

Expansion connector pinout descriptions:

Signal name	Description
PCIe_Exp1_T+	PCIe Lane 1
PCIe_Exp1_T-	
PCIe_Exp1_R+	
PCIe_Exp1_R-	
PCIe_Exp1_C+	
PCIe_Exp1_C-	
PCIe_Exp1_clkreq-(NC)	
PCIe_Exp2_T+ (NC)	PCIe Lane2. Not available in EmNANO i2300
PCIe_Exp2_T-(NC)	
PCIe_Exp2_R+(NC)	
PCIe_Exp2_R-(NC)	
PCIe_Exp2_C+(NC)	
PCIe_Exp2_C-(NC)	
PCIe_Exp2_clkreq-(NC)	
SATA-T+	SATA
SATA-T-	
SATA-R+	
SATA-R-	
AC_SDIN0	HD Audio Link
AC_BITCLK	
AC_SDOUT	
AC_RST#	
AC_SYNC	
I2C_Data	I2C interface
I2C_Clk	
USB2_D4_P	USB2.0 Interface
USB2_D4_N	
Host Reset-	Reset from Processor
+5V	5V supply from Carrier board
+3.3V	3.3V supply from Carrier board
Gnd	Digital ground

9 List of IO Connectors and Mating Cables

The following table provides a summary of all user-accessible I/O connectors on the board.

Function	Ref	Description	Mating Connector	DSC Mating Cable
Power in	J9	2x7 2mm pitch vertical pin header		6981070
USB 2.0	J1, J2	2x5 2mm pitch vertical pin header		6981082
USB 3.0	J4	2x6 2mm pitch vertical pin header		6980100
VGA	J3	2x5 2mm pitch vertical pin header		6981084
LVDS	J18	20 Positions Header Connector 0.039" (1.00mm) Surface Mount, Right Angle Tin		Custom
Serial Ports	J13, J14	2x5 2mm pitch vertical pin header		6981075
External battery	J6	2 pos. through-hole vertical shrouded pin header, 0.1” pitch	Molex Spox	6980524
GbE Ethernet	J11, J12	2x5 2mm pitch vertical pin header		6981080
Analog I/O	J10	2x13 2mm pitch vertical pin header		6980516
Digital I/O	J15	2x13 2mm pitch vertical pin header		6980516
PCIe Minicard / mSATA	J8	52-pin Minicard, full size		NA
Expansion Connector	J5	2x20 .635mm / .025” pitch SMD	Molex 53627-0474	NA
SD Card	J17	10 (8 + 2) Position Card Connector		NA

Table 1: Zeta board connector details

10 I/O Cables

The Zeta cable kit includes cables for all I/O features on Zeta except LCD. Details are provided below. Individual cables are available as a special order item. Minimum order quantities and lead times may apply.

An LCD / backlight cable kit is available for specific displays used in our manufacturing environment. Customers may purchase this cable kit as a starting point and modify the LCD ends to support their specific display.

No	Function	DSC cable no	Ref
1	Dual USB 2.0 cable (x2)	6981082	J1, J2
2	Dual Serial cable (x2)	6981075	J13, J14
3	External battery cable	6980524	J6
4	Ethernet cable (x2)	6981080	J11, J12
5-6	Analog I/O and Digital I/O cables	6980516	J10, J15
7	VGA cable	6981084	J3
8	Dual USB 3.0 (x1) cable	6980100	J4
9	Power input cable	6981070	J9

Table 2: Zeta board I/O cables

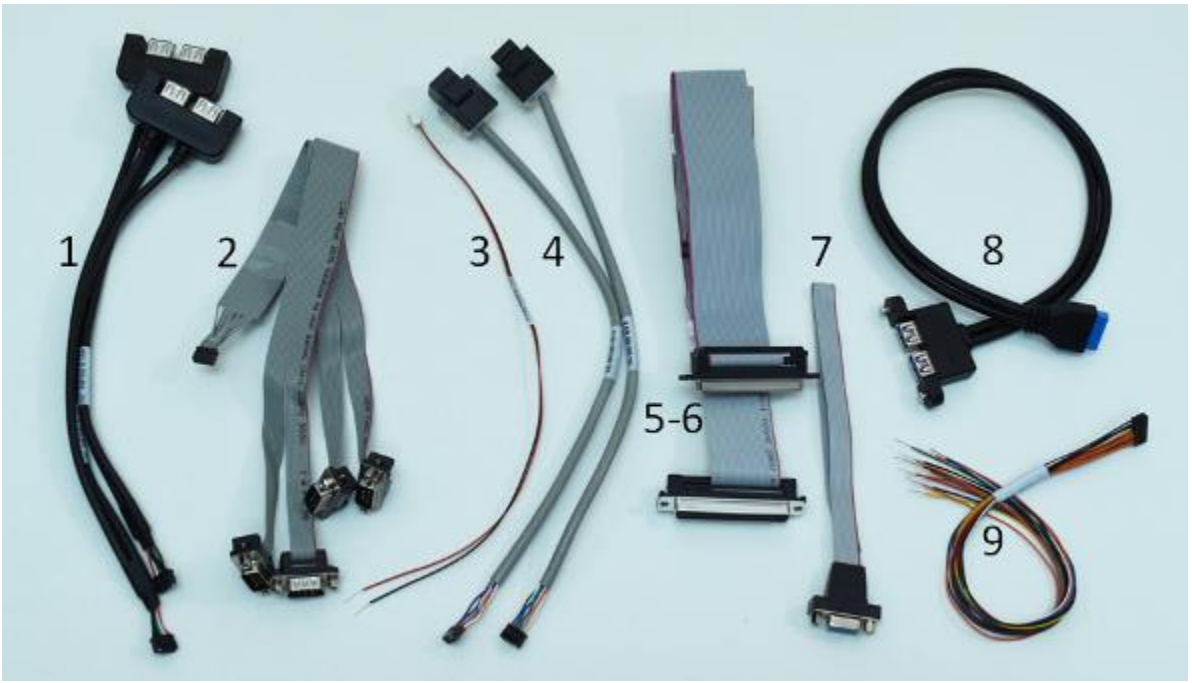


Figure 6: IO cables

11 Jumper Descriptions

The default jumper positions are shown in red.

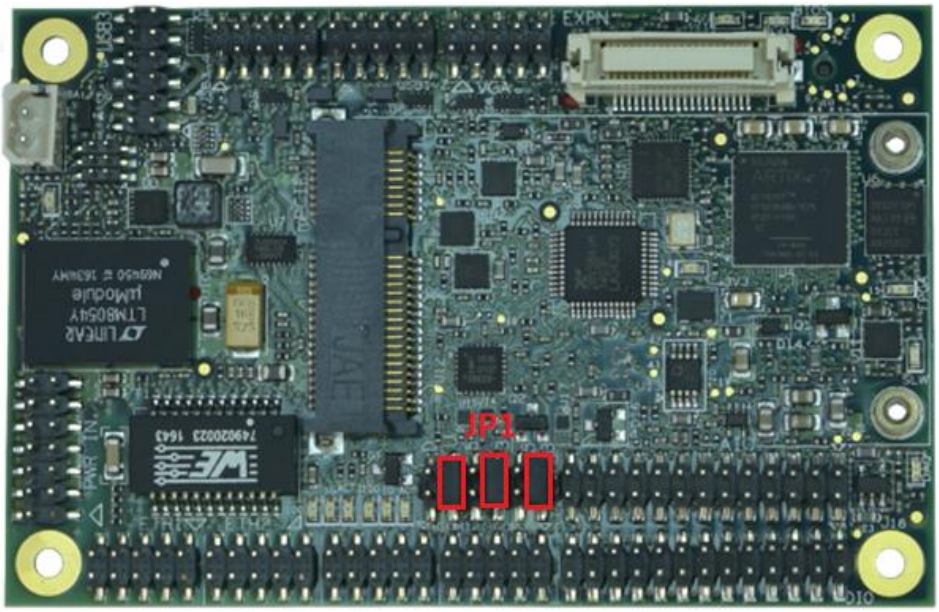


Figure 7: Zeta default jumper location

Jumper	Position	Description
JP1	1-2 3-4	LVDS PWM =3.3V LVDS PWM =5V
	5-6 7-8	VIO_DIO = 3.3V VIO_DIO = 5.0V
	9-10 11-12	DIO Pulled up DIO Pulled down

Table 3: Zeta board Jumper JP1 details

12 Zeta daughter board

12.1 Description

Zeta includes an expansion connector which supports the installation of a daughterboard with additional I/O and expansion features:

- Full/half-size MiniCard socket with PCIe x1 and USB2.0 connectivity
- M.2 M-keying SSD connector for 2242 size PCIe flash modules
- HD Audio with Line In, Mic In, Line Out
- 16 Digital IO lines with configurable 3.3V/ 5V logic levels and Pull-up/down resistors

12.2 Block Diagram

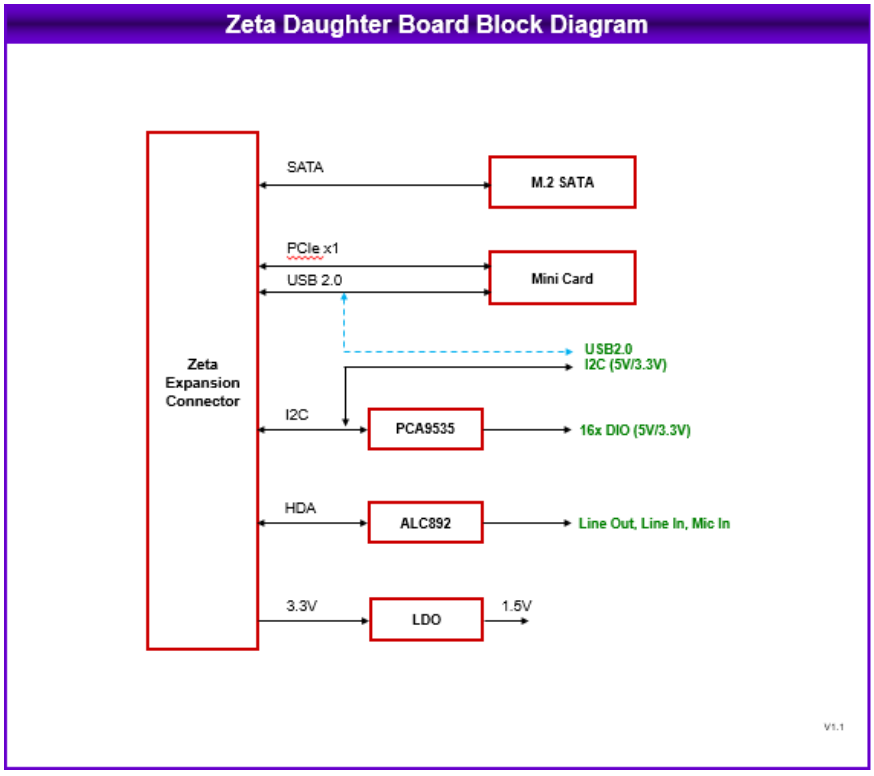


Figure 8 : Zeta daughter board block diagram

12.3 Mechanical, Electrical and Environmental

- Form factor 55 x 84 mm
- Cooling Not Applicable
- Power input No External Supply; 3.3V and 5V supplies via Expansion Connector
- Operating Temp -40°C to +85°C ambient

12.4 Feature Description

12.4.1 Expansion Connector

Zeta daughter board is interfaced to Zeta base board using 40 pin expansion connector. It supports the following interfaces.

- Two PCIe x 1 lanes
- HD Audio interface
- SATA interface
- USB2.0 interface
- I2C interface

*Second PCIe port will be unused in the daughter board.

12.4.2 Power Supply

Zeta daughter board is powered from 5V and 3.3V on the expansion connector. The 1.5V required for the PCIe Mini card socket is generated with a 3.3V to 1.5V LDO.

12.4.3 PCIe

PCIe lane 1 from the expansion connector is connected to PCIe Minicard socket; PCIe lane 2 from the expansion connector is unused. PCIe Minicard socket supports full-size PCIe Minicards. Two threaded spacers are mounted on the board for installing a full-size module. Mounting hole option for half-size module is also provided.

12.4.4 USB

USB 2.0 port 2 from the expansion connector is connected to PCIe Minicard socket. PCIe Minicard socket supports full-size Disk-On-Module. Option to route the same USB2.0 port to 2x5 header is provided.

12.4.5 Audio

Zeta daughter board supports HD audio using Codec ALC892GR.The Codec ALC892GR supports stereo line in, stereo line out and stereo mic in. These audio I/O signals are made available on a 2x5 header.

12.4.6 I2C

I2C interface from the expansion connector is connected to I2C expander PCA9535 for Digital IO expansion and same I2C routed to 2x5 header along with optional USB2.0 port. By default, voltage level of I2C will be 3.3V and onboard resistor jumper option is provided for 5V/3.3V selection.

I2C 7-bit address	Device	Board
0100 010	I2C IO expander PCA9535	Zeta base board
0100 011	I2C IO expander PCA9535	Zeta base board
0100 100	I2C IO expander PCA9535	Zeta daughter board

Table 4: I2C address

Note: Please contact DSC if there is an I2C address conflict

12.4.7 Digital IO

Zeta daughter board supports 16 Digital IOs via I2C expander PCA9535 on a 2x10 header. Jumper option to select 3.3V or 5V level and pull up/down option are provided.

12.4.8 LED Indicators

The board provides the following LED indicators. All LEDs are located near to board edge or their respective features. All LEDs are labeled in silkscreen with their function.

- One Green LED for Power Good indication
- Three Green LEDs for WWAN, WPAN, WLAN status signal indication from the PCIe Mini card connector

12.4.9 Jumper Configuration

The PCB design includes footprints to install 0-ohm resistors in place of all jumpers for a rugged configuration. All 0-ohm resistors are placed in logical positions compared to the pin headers.

Refer the below jumper settings to change the configuration for DIO signals.

Jumper Position	Configuration
1-2	VIO_DIO = 3.3V
2-3	VIO_DIO = 5V
4-5	DIO Pulled up
5-6	DIO Pulled down

Table 5: Zeta daughter board jumper details

12.5 Connector pinout and pin description

12.5.1 Expansion connector

Expansion connector pin outs are provided below.

+5V	1	2	+5V
PCIe_Exp2_T+ (NC)	3	4	PCIe_Exp1_T+
PCIe_Exp2_T-(NC)	5	6	PCIe_Exp1_T-
Gnd	7	8	Gnd
PCIe_Exp2_R+(NC)	9	10	PCIe_Exp1_R+
PCIe_Exp2_R-(NC)	11	12	PCIe_Exp1_R-
Gnd	13	14	Gnd
PCIe_Exp2_C+(NC)	15	16	PCIe_Exp1_C+
PCIe_Exp2_C-(NC)	17	18	PCIe_Exp1_C-
+3.3V	19	20	Gnd
SATA-T+	21	22	PCIe_Exp1_clkreq-(NC)
SATA-T-	23	24	PCIe_Exp2_clkreq-(NC)
+3.3V	25	26	USB2_D4_P
SATA-R+	27	28	USB2_D4_N
SATA-R-	29	30	Gnd
+3.3V	31	32	Host Reset-
AC_SDIN0	33	34	I2C_Data
AC_BITCLK	35	36	I2C_Clk
AC_SDOUT	37	38	AC_SYNC
AC_RST#	39	40	Gnd

Note: Pins with remark "(NC)" are not available with EmNANO i2300

12.5.2 Mini Card Socket

Mini card socket pin outs are provided below.

NC	1	2	+3.3V
NC	3	4	Gnd
NC	5	6	+1.5V
Clkreq-	7	8	NC
Gnd	9	10	NC
PCIe 1 Clk-	11	12	NC
PCIe 1 Clk+	13	14	NC
Gnd	15	16	NC
	KEY		
NC	17	18	Gnd
NC	19	20	Disable-
Gnd	21	22	PCIe Reset-
PCIe 1 RX-	23	24	+3.3V
PCIe 1 RX+	25	26	Gnd
Gnd	27	28	+1.5V
Gnd	29	30	SMB Clk
PCIe 1 TX-	31	32	SMB Data
PCIe 1 TX+	33	34	Gnd
Gnd	35	36	USB2_N

Gnd	37	38	USB2_P
+3.3V	39	40	Gnd
+3.3V	41	42	WWAN LED-
Gnd	43	44	WLAN LED-
NC	45	46	WPAN LED-
NC	47	48	+1.5V
Pull-up to +3.3V	49	50	Gnd
NC	51	52	+3.3V
Gnd	53	54	Gnd

Note: All TX/RX signals are with respect to the host. TX on the socket drives RX on the installed module, and RX on the socket is driven by TX on the installed module. The two mounting standoffs at the far end of the module installation site are not connected to ground.

12.5.3 M.2 SATA SSD Socket

M.2 SATA SSD socket pin outs are provided below.

Gnd	1	2	+3.3V
Gnd	3	4	+3.3V
NC	5	6	NC
NC	7	8	NC
NC	9	10	DAS/DSS#
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
NC	19	20	NC
Gnd	21	22	NC
NC	23	24	NC
NC	25	26	NC
Gnd	27	28	NC
NC	29	30	NC
NC	31	32	NC
Gnd	33	34	NC
NC	35	36	NC
NC	37	38	DEVSLP
Gnd	39	40	NC
SATA_RX+	41	42	NC
SATA_RX-	43	44	NC
Gnd	45	46	NC
SATA_TX-	47	48	NC
SATA_TX+	49	50	NC
Gnd	51	52	NC
NC	53	54	NC
NC	55	56	NC
Gnd	57	58	NC
	KEY		
NC	67	68	NC
Gnd	69	70	+3.3V
Gnd	71	72	+3.3V
Gnd	73	74	+3.3V
Gnd	75		

Note: All TX/RX signals are with respect to the host. TX on the socket drives RX on the installed module, and RX on the socket is driven by TX on the installed module. One mounting standoffs at the far end of the module installation site are not connected to ground.

12.5.4 Audio

Audio connector pinouts are provided below.

LineOut-L	1	2	LineOut-R
GND_Audio	3	4	GND_Audio
LineIn-L	5	6	LineIn-R
GND_Audio	7	8	GND_Audio
MIC_L	9	10	MIC_R

12.5.5 Digital I/O

Digital I/O connector pinouts are provided below.

+5V/3.3V	1	2	DIO A0
DIO A1	3	4	DIO A2
DIO A3	5	6	DIO A4
DIO A5	7	8	DIO A6
DIO A7	9	10	DIO B0
DIO B1	11	12	DIO B2
DIO B3	13	14	DIO B4
DIO B5	15	16	DIO B6
DIO B7	17	18	NC
Dground	19	20	Dground

12.5.6 USB-I2C header

USB I2C header pinouts are provided below.

NC	1	2	NC
Gnd	3	4	Gnd
USB2+	5	6	I2C CLK
USB2-	7	8	I2C DATA
USB_5V	9	10	**3P3**/5V0

12.6 Connector and cable Information

12.6.1 Connector Table

The following table provides a summary of all I/O connectors on the board.

Function	Reference	Description	DSC Mating Cable
Digital I/O	J15	2x10, 2mm pitch, SMT Header	
Audio	J25	2x5, 2mm pitch, SMT Header	6981076
PCIe Minicard	J24	52-pin Minicard, full size, with PCB mount threaded spacers	NA
M.2 SSD socket	J8	75-pin M.2 M keyed socket, 2242, with PCB mount threaded spacer	NA
Expansion Connector	J7	Conn 40POS Vertical mount .635mm SMD	NA

Table 6: Zeta daughter board connectors

12.7 Mechanical Board Drawing of Zeta daughter board

The form factor of Zeta daughter board is COM express Nano Type 10 with dimensions 55 x 84 mm.

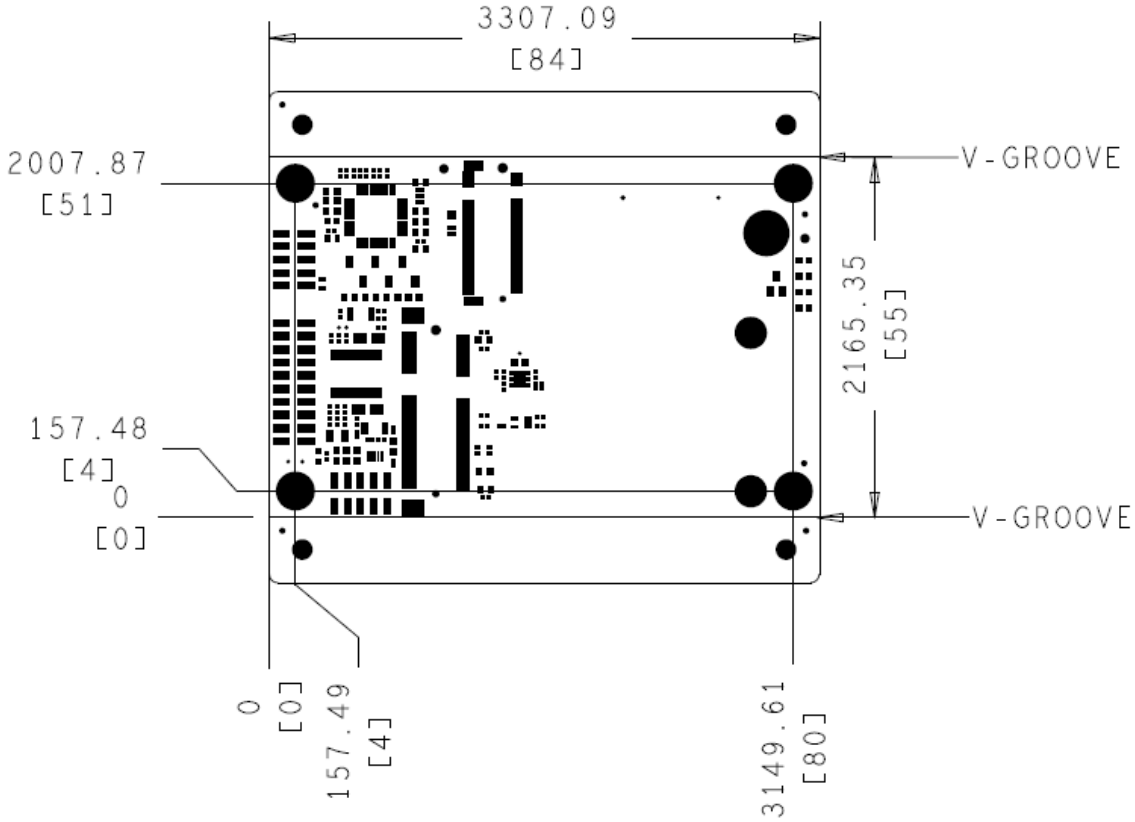


Figure 9: Mechanical outline top view

12.8 Connector and jumper location

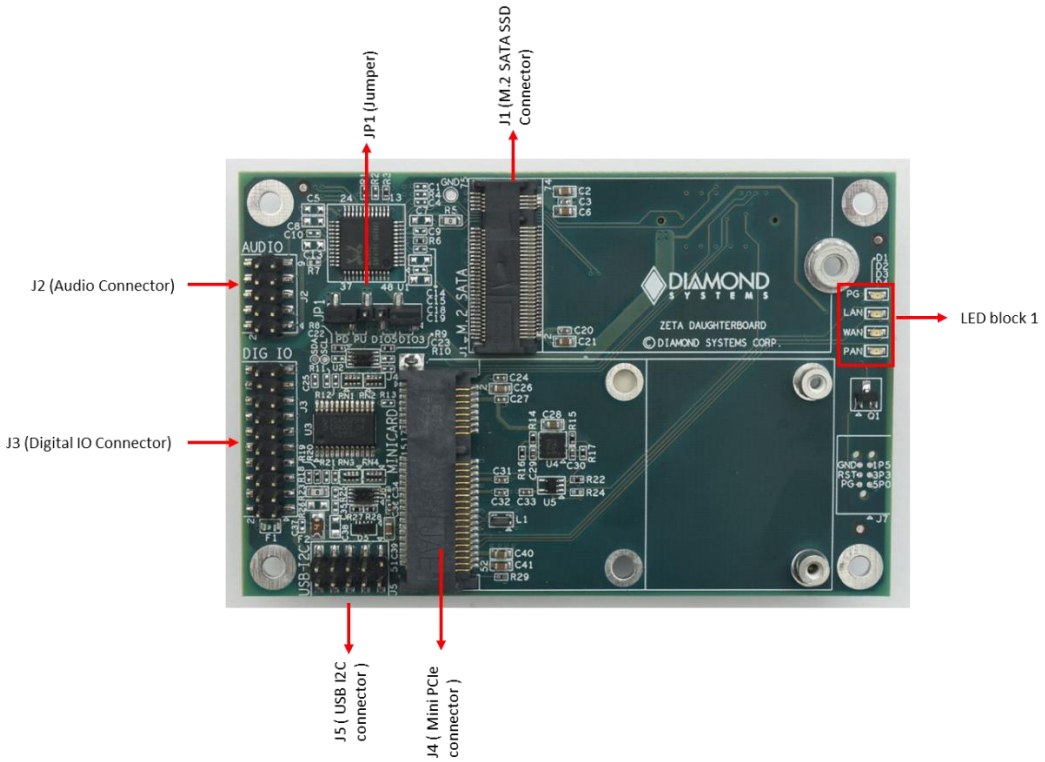


Figure 10: Zeta daughter board connectors and jumpers – Top side

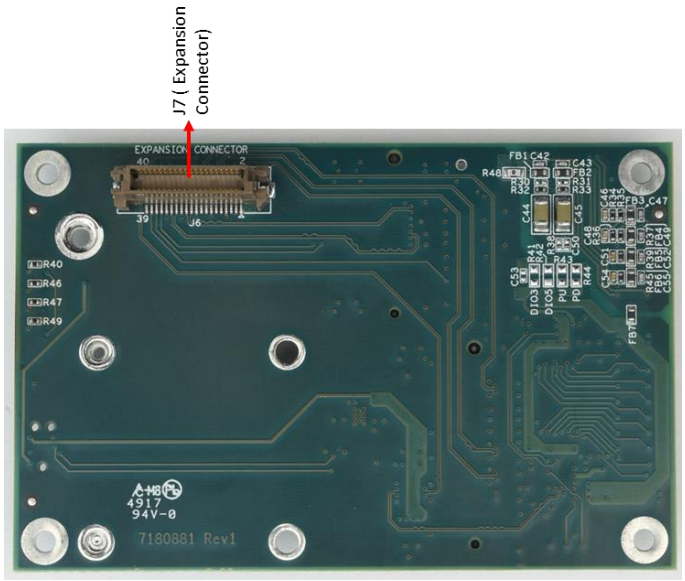


Figure 11: Zeta daughter board connectors– Bottom side

13 Mass storage

Systems which do not require any additional I/O beyond the baseboard features may use the baseboard's MiniCard/mSATA socket to contain the system bootable mass storage. For Linux operation, the Micro SD socket may also be used for mass storage, leaving the MiniCard socket available for expansion. A system running Windows must use the minicard/mSATA socket for the boot device, so if additional I/O is needed, the Zeta daughterboard can be used. In this case the designer has the choice of either the baseboard mSATA socket or the daughterboard' s M.2 socket for the bootable mass storage. If the M.2 socket is used, then both the baseboard and the daughterboard minicard sockets are available for I/O module installation.

13.1 List of options

Diamond Systems offers the following extended temperature mSATA or M.2 flash disks for use with Zeta.

Model Number	Description
FDMM-64G-XT	64GB mSATA MLC Flashdisk
FDMM-32G-XT	32GB mSATA MLC Flashdisk
FDMM-16G-XT	16GB mSATA MLC Flashdisk
FDMS-64G-XT	64GB mSATA SLC Flashdisk
FDMS-32G-XT	32GB mSATA SLC Flashdisk
FDMS-16G-XT	16GB mSATA SLC Flashdisk
FDMS-8G-XT	8GB mSATA SLC Flashdisk
TBD	M.2

13.2 Installation and configuration

To install any of the above SATA flash disk devices, locate the desired mSATA (J8) port Zeta base board or M.2 socket(J1) on Zeta daughter board ports. Plug the flash disk module into the appropriate port. Remove the screw(s) from the mounting stand-off(s) before installing the flash disk. Install the flash disk and secure it to the Zeta base board/daughter board with the screw(s) once the flash disk is installed.

14 "A" Model Data Acquisition Circuit

Zeta is available in two configurations. Both configurations are available with any processor option.

- The "D" model provides 16 GPIO lines with 3.3V/5V logic compatibility and jumper-selectable pull-up/down resistors.
- The "A" model features a comprehensive data acquisition circuit providing 16 SE / 8 DI analog inputs with +/-10V, +/-5V, 0-10V, and 0-5V input ranges, 100KHz max sample rate with2048-sample FIFO, 4 analog outputs with 0-5V and 0-2.5V ranges, 27 GPIO instead of 16, 4 32-bit counter/timers, and 4 24-bit PWMs.

The circuit controller is an FPGA that interfaces to the processor via the LPC bus from the COM express connector.

A/D Features

- 16 analog voltage inputs
- 16-bit resolution (1 part in 65536)
- Programmable input ranges: 0-5V, 0-10V, +/-5v, +/-10V
- Single-ended and differential input configuration options
- Precision, low-drift 2.5V reference voltage
- 100KHz maximum total A/D sample rate (all active channels combined)
- Integrated 2048-sample FIFO and interrupt service for efficient high-speed sampling

D/A Features

- 4 analog voltage outputs
- 16-bit resolution (1 part in 65536)
- Single-channel and multi-channel simultaneous update modes
- Programmable output range: 0-5V, 0-2.5V
- 30KHz update rate capability
- Waveform generator on 1 to 4 outputs with user-defined waveforms and 2048-sample waveform buffer

Digital I/O features

- 27 digital I/O lines
- User-selectable 3.3V / 5V logic levels
- User-selectable 10K pull-up / pull-down resistors
- Programmable direction in 8-bit and 1-bit groups
- 8-bit programmable edge detection circuit
- Buffers for protection and higher current drive
- 8 32-bit counter/timers with up counting, down counting, pulse output, and interrupt features
- 4 24-bit pulse-width modulators with programmable duty cycle and output polarity
- Interrupt support on ISA bus for A/D, digital I/O, and counter/timer circuits

All digital and analog I/O features are supported by Diamond's industry-leading Universal Driver software, which provides a C language programming library that supports all features in an easy-to-use, high-level fashion. A graphical monitor and control program provides easy access to all the I/O features and lets you prototype your application quickly as well as debug problems. Universal Driver is available as a free download from our website upon acceptance of our software license agreement.

14.1 Block Diagram

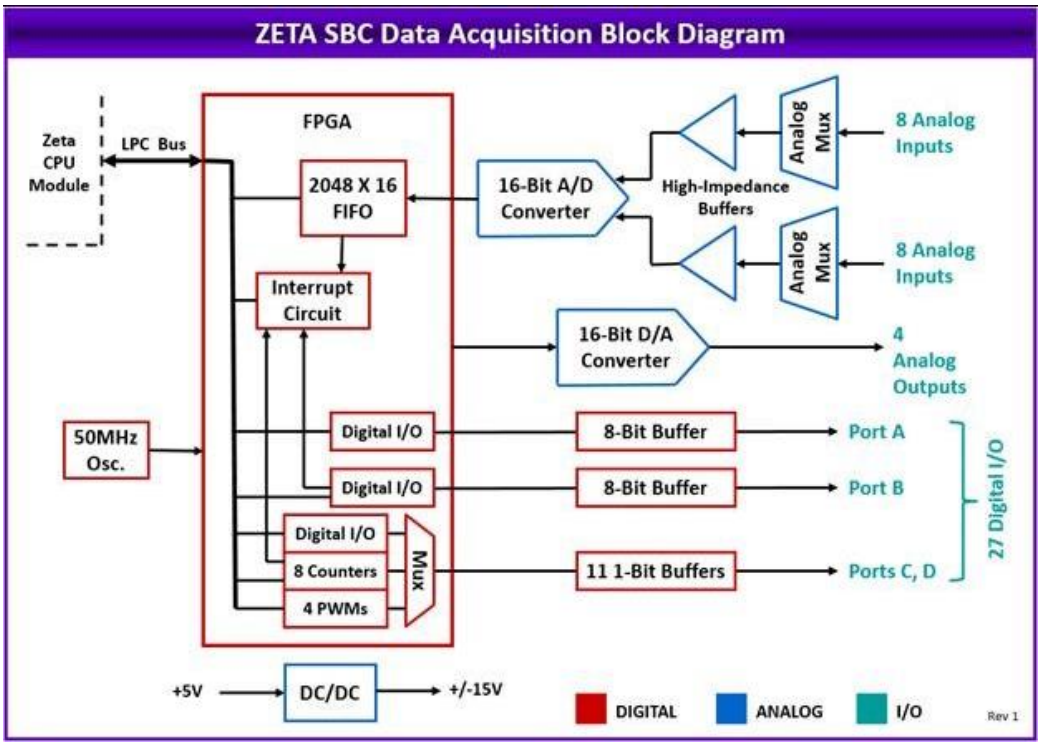


Figure 12: Data Acquisition Circuit Block Diagram

14.2 Analog-to-Digital Circuit

14.2.1 A/D Circuit Overview

Zeta base board "A" models include an analog input circuit based on the LTC1859 16-bit A/D converter, or ADC. The LTC1859 is capable of operating at up to 100,000 samples per second in total, either on a single channel or on any number of channels. The ADC supports programmable input ranges of 0-5V, 0-10V, +/-5V, and +/-10V. The input range can be changed on a sample by sample or channel by channel basis.

The LTC1859's performance is improved by the addition of several external components. The LTC1859 includes a built-in channel multiplexor. However, this multiplexor is bypassed in order to use an external circuit with increased channel count and higher input impedance. One pair of input channels is fed by two 8-channel multiplexors that can be configured for either 16 single-ended or 8 differential inputs. The ADC voltage reference is driven by an external precision 2.5V reference chip with higher initial accuracy and lower temperature drift than the LTC1859's built-in reference. This helps to reduce gain errors in A/D measurements.

In single-ended mode, each channel is measured with respect to analog ground, i.e. the input signal must be connected between the input pin and the analog ground pin on the I/O connector. In differential mode, the voltage is measured as the difference between the two input pins, and the analog ground pin is not part of the measurement. When operating in single-ended mode, the two native input channels are expanded to 16 single-ended channels, and when operating in differential mode, the two channels are expanded to 8 differential channels.

14.2.2 A/D Channel Selection, Sampling, and Timing

A/D conversions may be triggered by several sources, including a software command, a programmable clock in the circuit's FPGA, and an external digital signal connected to one of the board's digital I/O ports. These options provide maximum flexibility in tailoring the circuit's performance to a wide variety of real-world applications. Software triggering is mostly used for low-speed sampling needs or where the exact elapsed time between samples is not critical. External triggering is used when the A/D sampling must be synchronized to some external

activity such as a rotary or linear encoder. Clock timing is used for high speed sampling or where the time between samples must be precise.

A channel sequencer circuit in the FPGA controls which channels sampled by the ADC. The sequencer can be programmed to select any single channel repeatedly, or it can be programmed to select any consecutive group of channels. As described above, the A/D front end consists of two 8-channel multiplexors connected to two analog inputs of the ADC. In single-ended mode, the channel sequencer will treat the 16 inputs as channels 0-15 with reference to analog ground, and in differential mode the sequencer will treat them as 8 differential channels, with channels 0-7 forming the high side of the inputs (renamed as channels 0+ to 7+) and channels 8-15 forming the low side of the inputs (renamed as channels 0- to 7-).

The sequencer works in conjunction with two available sampling modes called sample and scan. In sample mode, each A/D clock or trigger event causes one A/D conversion to occur. If the sequencer is programmed for a single channel, each successive A/D conversion will sample the same channel. This method is useful for high speed sampling of an AC signal. If the sequencer is programmed for a range of channels, then each successive A/D clock will cause the next channel in the selected range to be sampled, with the result that all the selected input channels are sampled one at a time in round robin fashion.

In scan mode, each A/D clock generates one A/D conversion on all channels selected by the sequencer (called the scan range) in tight succession. This method is typically used with the programmable clock circuit to measure a group of channels all at once. The number of selected channels is called the scan size. The timing of scan mode differs significantly from sample mode in that all selected channels are sampled as closely together as possible in time instead of being spread out equally in time as is done in sample mode. The analog input circuit does not support simultaneous sampling mode, where all inputs are sampled at exactly the same time.

One very important fact to remember is that because scan sampling generates one A/D conversion for every channel in the scan range, the total sample rate of the circuit is equal to the clock rate times the scan size. This total sample rate must be kept at or below the hard 100KHz limit of the A/D converter.

A second very important fact is that the fastest possible sample rate for any channel is 100KHz divided by the scan size in scan mode or the number of selected channels in sample mode. Thus it is not possible to sample more than one channel at 100KHz. If two channels are selected, the maximum sample rate for each channel is 50KHz, and so on.

14.2.3 A/D FIFO and High Speed Sampling

The FPGA contains a 2048 sample FIFO which supports high-speed A/D sampling. The FIFO enables the CPU to avoid having to respond every time an A/D conversion occurs, which would consume too much processor time when high speed sampling is being executed. Instead, the A/D samples are stored in the FIFO, and when the number of samples reaches a user-defined threshold, an interrupt occurs on the ISA bus. The software can then respond to the interrupt and read out a large number of samples all at once.

The Diamond Systems Universal Driver software provides full support for high speed A/D sampling with FIFO and interrupt support. Please refer to that user manual for operating details. When using Universal Driver software, the interrupt rate is equal to the total A/D sample rate divided by the programmed FIFO threshold, because each time the interrupt service routine runs, it will read out the number of samples equal to the threshold value. The threshold is programmable so that the application software can optimize the interrupt rate for its needs. In general the interrupt rate should not exceed 1KHz, and in most cases an interrupt rate of 100-200Hz is recommended.

14.2.4 A/D Operation

In essence, an A/D converter converts an analog voltage to a number that indicates the ratio between that voltage and the full range of voltages that the A/D can measure. A 16-bit A/D converter means that all input voltages are represented by a 16-bit binary number ranging from 0 to 65535 (2^{16}-1), or binary 0000 0000 0000 0000 to 1111 1111 1111 1111. There are two groups of input ranges, unipolar and bipolar. Unipolar ranges consist of only positive voltages (0-5V, 0-10V), and bipolar ranges include both negative and positive voltages (+/-5V, +/-10V). For a unipolar input range, the A/D values are straight binary and will range from 0 (binary 0000 0000 0000 0000) for 0V to 65535 (binary 1111 1111 1111 1111) for the top end of the range. For a bipolar input range, the A/D values are 2s complement and will range from -32768 (binary 1000 0000 0000 0000) to +32767 (binary 0111 1111 1111 1111).

The tables below summarize the relationship between input voltage and A/D values for the general case. Note that the nominal upper limit of the input range (5.0000V or 10.0000V) is not achievable, since this voltage would require a 17 bit number (2^{16} or 1 0000 0000 0000 0000). V_{FS} means the full-scale input voltage, either 5V or 10V.

Bipolar Input Ranges

A/D Code	A/D code binary	Formula	+/-5V input range	+/-10V input range
-32768	1000 0000 0000 0000	$-V_{FS}$	-5.0000V	-10.0000V
-32767	1000 0000 0000 0001	$-V_{FS}$ + 1 LSB	-4.9998V	-9.9997V
-1	1111 1111 1111 1111	-1 LSB	-0.153mV	-0.305mV
0	0000 0000 0000 0000	0V	0.0000V	0.0000V
1	0000 0000 0000 0001	+1 LSB	0.153mV	.305mV
32767	0111 1111 1111 1111	V_{FS} - 1 LSB	4.9998V	9.9997V

Unipolar Input Ranges

A/D Code	A/D code binary	Formula	0-5V input range	0-10V input range
0	0000 0000 0000 0000	0V	0.0000V	0.0000V
1	0000 0000 0000 0001	1 LSB (V_{FS} / 65536)	0.076mV	0.153mV
32767	0111 1111 1111 1111	V_{FS} / 2 - 1 LSB	2.4999V	4.9998V
32768	1000 0000 0000 0000	V_{FS} / 2	2.5000V	5.0000V
32769	1000 0000 0000 0001	V_{FS} / 2 + 1 LSB	2.5001V	5.0002V
65535	1111 1111 1111 1111	V_{FS} - 1 LSB	4.9999V	9.9998V

14.2.5 A/D Resolution

The smallest change in input voltage that can be detected is 1/(2^{16}), or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and is referred to as 1 LSB (1 Least Significant Bit). The resolution is always 16 bits, but the value of 1 LSB will vary with the input range.

Polarity	*Input Range*	*Resolution (1LSB)*
Bipolar	±10V	305µV
Bipolar	±5V	153µV
Unipolar	0 - 10V	153µV
Unipolar	0 - 5V	76µV

14.2.6 Input Range Selection

The input range of the A/D circuit is programmable in software and can be selected from the 4 values shown in the table above. Refer to the Universal Driver software user manual A/D section for details. The input range can be changed anytime, so that you can use different ranges for different input signals based on the best match. In general, you should select the highest gain (smallest input range) that allows the A/D converter to read the full range of voltages over which the input signals will vary. For example, if you have a signal that ranges from 0V minimum to 3V maximum, use the 0-5V range for best resolution. An input range that is too small causes the A/D converter to clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

14.2.7 Converting A/D Readings to Volts or Engineering Units

The A/D always returns a 16-bit binary number that represents the value of the input voltage relative to the selected input range. This number needs to be converted to a meaningful value in order to be used in your application. The first step is to convert it back to the actual measured voltage. Afterwards, you may need to convert the voltage to some other engineering units such as temperature in degrees C or weight in grams.
Since there are many possible formulas for converting the input voltage to engineering values, this secondary step is not described here. Only conversion to input voltage is described. However, you can combine both voltage and engineering unit conversions into a single formula if desired.

To convert the A/D value to its corresponding input voltage, use the following formulas.

Conversion Formula for Bipolar Input Ranges

Input voltage = A/D value / 32768 * Full-scale input voltage

where the A/D value is a 2s complement number ranging from -32768 to 32767, and the full-scale voltage is the nominal maximum value, either 5V or 10V.

Example:
For bipolar input range ±5V, full-scale input voltage = 5V
For an A/D value of 17761: Input voltage = 17761 / 32768 * 5V = 2.710V
For an A/D value of -12345: Input voltage = -12345 / 32768 * 5V = -1.884V

Conversion Formula for Unipolar Input Ranges

Input voltage = A/D value / 65536 * Full-scale input voltage

where the A/D value is a straight binary number ranging from 0 to 65535, and the full-scale voltage is the nominal maximum value, either 5V or 10V.

Example:
For unipolar input range 0-5V, full-scale input voltage = 5V.
For an A/D value of 17761: Input voltage = 17761 / 65536 * 5V = 1.355V

14.2.8 Measurement Accuracy and Calibration

Although the A/D circuit has 16-bit resolution (meaning it can resolve input voltages to within $1/2^{16}$ or 1/65536 of its input range), The measurement accuracy is not necessarily the same. All A/D circuits exhibit two inherent errors known as offset and gain errors. In addition, all A/D circuits will experience some minor drift as the ambient temperature changes, as well as lesser drift over long periods of time.

To minimize the size and cost of the A/D circuit while still providing reasonable performance, the A/D circuit on Zeta base board does not provide calibration features to eliminate these errors. Instead the circuit was designed to minimize the inherent offset, gain, and drift characteristics. The specifications at the end of this manual indicate the worst-case offset, gain, and temperature drift errors in the circuit. Most boards will exhibit errors much lower than these values (typically 25-50% of the published values), so the A/D measurements can typically be used satisfactorily in your application without concern.

If higher accuracy is required, a software or digital calibration technique can be implemented in your application. Measure two known voltages close to the lower and upper limits of the input range you are using. The ideal values are between 1% and 5% at the bottom end and 95% and 99% at the top end. Compare the actual A/D readings of these input voltages to the expected values, and then store the differences in a file. Then you can use these errors to apply an offset and gain factor to each A/D reading on that board forevermore. Although this technique does not eliminate temperature and drift errors, it will eliminate the largest portion of the total error and provide more accurate measurements and better overall product performance.

When considering accuracy, it is important to consider all the contributions to measurement error. In addition to the inherent A/D errors, the sensors connected to the A/D also have their own offset, gain, and temperature/time drift errors. Usually these errors will be published as a simple accuracy figure in a percentage form. One percent error on a 16-bit A/D is 655 LSBs, so if your sensor has a 1% error specification, that is already more than 10x the typical A/D reading error, and therefore software calibration of the A/D readings alone will not provide any material benefit. However, the same technique described above can be applied with the sensor connected using known input conditions (for example empty scale and scale with a precision weight applied), so that you can eliminate total system error.

To include A/D error values into the input voltage calculation, use this formula:

Input voltage = ((ADC – Cmin) / (Cmax – Cmin)) * (Vmax – Vmin) + Vmin

ADC = A/D code
Vmax = Test input voltage at top end of A/D scale used in calibration procedure
Vmin = Test input voltage at bottom end of A/D scale used in calibration procedure
Cmax = A/D code at Vmax input
Cmin = A/D code at Vmin input
This formula works for both unipolar and bipolar input ranges.

14.2.9 Input Impedance

Another factor that can significantly affect A/D measurement accuracy is the ratio between the input impedance of the A/D circuit and the output impedance of the signal being measured. The voltage seen by the A/D converter is a simple resistor divider between the two impedances, with the input signal at the top of the divider and the A/D in the middle. The higher the output impedance of the input signal, the greater the error will be. Conversely, the higher the input impedance of the A/D circuit, the lower the error will be. Zeta base board uses high impedance, ultra-low-offset buffer op amps to boost the input impedance to well over 10 GigOhms (the input impedance is calculated based on the specified input current of 75pA). This ensures that the source impedance of any expected input signal will not have any material effect on the A/D readings.

14.3 Digital-to-Analog Circuit

14.3.1 Overview

The Zeta base board data acquisition circuit uses a 16-bit D/A converter. This means that all output voltages are defined by a 16-bit binary number, or D/A code, ranging from 0 to 65535 (2^{16}-1), or binary 0000 0000 0000 0000 to 1111 1111 1111 1111. The Zeta base board D/A circuit supports only unipolar output voltage ranges (positive voltages only). For a unipolar output range, the D/A codes are straight binary and will range from 0 (binary 0000 0000 0000 0000) for 0V to 65535 (binary 1111 1111 1111 1111) for the top end of the range.

The tables below summarize the relationship between D/A codes and output voltages. Note that the nominal upper limit of the output range (5.0000V or 2.5000V) is not achievable, since this voltage would require a 17-bit number (2^{16} or 1 0000 0000 0000 0000). V_{FS} means the full-scale output voltage, either 5V or 2.5V.

D/A Output Codes to Output Voltages

D/A Code	D/A code binary	Formula	0-5V output range	0-2.5V output range
0	0000 0000 0000 0000	0V	0.0000V	0.00000V
1	0000 0000 0000 0001	1 LSB (V_{FS} / 65536)	0.0763mV	0.0381mV
32767	0111 1111 1111 1111	V_{FS} / 2 - 1 LSB	2.4999V	1.24996V
32768	1000 0000 0000 0000	V_{FS} / 2	2.5000V	1.25000V
32769	1000 0000 0000 0001	V_{FS} / 2 + 1 LSB	2.5001V	1.25004V
65535	1111 1111 1111 1111	V_{FS} - 1 LSB	4.9999V	2.49996V

14.3.2 D/A Resolution

The smallest change in output voltage that can be obtained is 1/(2^{16}), or 1/65536, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code and is therefore referred to as 1 LSB (1 Least Significant Bit). The D/A resolution is always 16 bits, but the value of 1 LSB will vary with the output range.

Polarity	*Output Range*	*Resolution (1LSB)*
Unipolar	0 - 5V	76.3µV
Unipolar	0 – 2.5V	38.1µV

14.3.3 Output Range Selection

The output range of the D/A circuit is programmable in software and can be selected from the 2 values shown in the table above. Refer to the Universal Driver user manual D/A functions for details. The output range can be changed anytime. However, unlike the A/D circuit, changing the output range affects all output channels simultaneously. In general, you should select the smallest output range that allows the D/A converter to cover the full range of output voltages you need for your application. For example, if you need the output to vary from 0V minimum to 2V maximum, use the 0-2.5V output range for best resolution. Note that the Zeta base board D/A circuit cannot output negative voltages.

14.3.4 D/A Conversion Formula

The D/A code written to the D/A circuit is always a straight binary integer ranging between 0 and 65535 (2^{16}-1). You may choose to round up or down to achieve the most accurate output value.
To calculate the required D/A code for the desired output voltage:

D/A code = (Desired output voltage / Full scale voltage) * 65536

where Full scale voltage is either 5V or 2.5V depending on the selected output range.
To determine the output voltage resulting from a given D/A code:

Output voltage = (D/A code / 65536) * Full scale voltage

Examples:
For unipolar output range 0-5V, full-scale voltage = 5.000V.
For a desired output voltage of 1.000V: D/A code = (1.000V / 5.000V) * 65536 = 13107

For unipolar output range 0-2.5V, full-scale voltage = 2.500V.
For a desired output voltage of 1.000V: D/A code = (1.000V / 2.500V) * 65536 = 26124

14.3.5 Output Accuracy and Calibration

Although the D/A circuit has 16-bit resolution (meaning it can resolve output voltages to within $1/2^{16}$ or 1/65536 of its output range), The output accuracy is not necessarily the same. As with A/D circuits described earlier, all D/A circuits exhibit two inherent errors known as offset and gain errors. In addition all D/A circuits will experience some minor drift as the ambient temperature changes, as well as lesser drift over long periods of time.

To minimize the size and cost of the D/A circuit while still providing reasonable performance, the D/A circuit on Zeta base board does not provide calibration features to eliminate these errors. Instead the circuit was designed to minimize the inherent offset, gain, and drift characteristics. The specifications at the end of this manual indicate the worst-case offset, gain, and temperature drift errors in the circuit. Most boards will exhibit errors much lower than these values (typically 25-50% of the published values), so the D/A can typically be used satisfactorily in your application without concern.

If higher accuracy is required, a software or digital calibration technique can be implemented in your application. Write the bottom and top output codes (0 and 65535) to the D/A circuit and measure the actual output voltages. Compare the actual voltages to the expected values, and then store the differences in a file. Then you can use these errors to apply an offset and gain factor to the D/A conversion formula that board forevermore. Although this technique does not eliminate temperature and drift errors, it will eliminate the largest portion of the total error and provide more accurate measurements and better overall product performance.

When considering accuracy, it is important to consider the requirements of your application. In many applications, 16-bit resolution is better than the system requires for proper operation. For example, if you are controlling the brightness of a lamp viewed by the human eye, a resolution of 8 bits (1/256) would probably be sufficient in most scenarios. D/A errors only need to be considered if they will have a material impact on the performance of your application.

To incorporate error measurements into the D/A code calculation, use this formula:

D/A code = max((Target voltage – Vmin) / (Vmax – Vmin) * 65535), 0)

Target voltage = the desired output voltage
Vmin is the voltage measured with D/A code 0
Vmax is the actual output voltage with D/A code 65535

Examples for 0-5V output range:
offset voltage = .003V, full-scale voltage = 5.012V, desired output voltage = 1.000V
D/A code = (1V - .003V) / (5.012V - .003V) * 65535 = **13044**
offset voltage = -.003V, full-scale voltage = 4.996V, desired output voltage = 1.000V
D/A code = (1V + .003V) / (4.996V - .003V) * 65535 = **13149**
Note: In this formula, the binary code scale value is 65535, not 65536. This is because the full scale voltage Vmax was measured with the actual output code of 65535.
Note: The output values are limited to voltages between the 0 code voltage and the 65535 code voltage. If the offset voltage is positive, you cannot output 0V.
Note: D/A codes are limited to positive values in the range 0-65535. Therefore, a positive offset voltage (output voltage is greater than zero when D/A code = 0) cannot be corrected, since correction would require a D/A code less than zero. This is why the formula above uses the max() function to force a minimum D/A code of zero.

14.4 Digital I/O Features

14.4.1 Overview

The 27 digital I/O lines are organized as 4 ports A, B, C, and D. Ports A, B, and C are 8 bits wide, and port D is 3 bits wide. All ports may be configured with a jumper for either 3.3V or 5V logic levels, and all ports may also be configured with a jumper for 10K ohm pull-up or pull-down resistors. These settings apply to all ports collectively; it is not possible to configure some ports for 3.3V and others for 5V at the same time, or to configure some ports for pull-up and other ports for pull-down simultaneously.

All digital I/O ports utilize logic buffers (transceivers) to provide enhanced output current capability and protect the FPGA from faulty connections. Ports A and B utilize 8-bit transceivers, and their directions are set for all 8 bits as a group. Ports C and D utilize 1-bit transceivers, and their directions are individually configurable for each bit. For safety and to prevent glitches, on power up or reset, all ports reset to input mode and all port data registers reset to all 0.

All DIO ports may operate in “normal” digital I/O mode where they are written and read directly with their data registers. In addition to normal mode, port B may be used for edge detection. If the input value of any bit on port B changes, that change can drive an interrupt, which will then cause user-specified code to run. Ports C and D may also be configured to support other features on the board, such as counter/timer I/O, PWM output, and analog circuit triggers.

“A” Model Digital I/O Summary

Port	*Size*	*Direction control*	*Special features*
A	8 bits	Bytewise	N/A
B	8 bits	Bytewise	Edge detect capability
C	8 bits	Bitwise	Counter and PWM I/O
D	3 bits	Bitwise	A/D external clock D/A waveform external clock

14.4.2 Edge Detection Circuit

On “A” models, an edge detection circuit is available on port B. The edge detection circuit can be used to notify the processor when a particular event occurs, such as a door opening, a switch being pressed, or a light curtain being penetrated.

The edge detection circuit on Zeta contains an enable register, a polarity register, and a status register. The programmer can specify which bits will be active with the enable register and which transition to detect on each bit (0 to 1 or 1 to 0) with the polarity register. The status register indicates which bits have seen the specified change since the last time it was read. The programmer provides custom code to define the functionality to be performed whenever specified edges occur. When a qualifying edge occurs, the circuit will generate an interrupt on the ISA bus. If the Diamond Universal Driver software is being used, the driver will respond to the interrupt and pass control to the user's custom code. After executing the application-specific functionality, the custom code must clear the interrupt request in order to be ready for the next event.

14.4.3 Support for Special Functions

On "A" models, port C and D bits may be defined as inputs or outputs for the 8 counter/timers as well as outputs for the 4 PWMs, as indicated below. Configuring these features is explained in the following sections and in the Diamond Universal Driver user manual.

DIO Bit	*Alternate Signal*
C0	Counter 0 I/O
C1	Counter 1 I/O
C2	Counter 2 I/O
C3	Counter 3 I/O
C4	Counter 4 I/O, PWM 0 out
C5	Counter 5 I/O, PWM 0 out
C6	Counter 6 I/O, PWM 0 out
C7	Counter 7 I/O, PWM 0 out
D1	D/A waveform external trigger
D2	A/D external trigger

14.4.4 Power Pins

The digital I/O connector J17 contains a pin capable of supplying a digital power supply voltage for user convenience. The voltage is determined by the digital I/O logic level jumper and is either 3.3V or 5.0V. The pin is protected by a resettable PTC (positive temperature coefficient) fuse with a 100mA maximum steady state current rating. If the current on this pin exceeds ~100mA (typically due to a short or overcurrent condition), the fuse will heat up and turn into a high impedance, causing the output voltage and current to drop to a trickle level, which is just enough to maintain the fuse in the high temperature blocking mode. This blocking condition can persist indefinitely without causing damage to the component or the board. Once the short or overcurrent condition is removed, the fuse will cool down in approximately 1-2 seconds, and the pin will return to its normal voltage and current capacity.

The digital I/O connector also contains a digital ground pin, which should serve as the reference and current return paths for all digital I/O connections on J17. This pin does not have fuse protection; however its safe operating limit is 1.0A.

14.5 Counter/Timer Features

14.5.1 Overview

Zeta "A" models include 8 32-bit counter/timers with a wide array of features and programmability. Both up and down counting are supported, and the clock for each counter can be selected from an internal 50MHz or 1MHz clock or an external digital signal. In down counting mode, an optional programmable-width output pulse may be enabled each time the counter reaches zero. Counters can also be used to generate programmable interrupts on the ISA bus, enabling custom code to be run at precise user-defined intervals.

14.5.2 Counter Commands

The counters are configured and managed with a series of commands. These commands are implemented in the Diamond Systems Universal Driver software. Commands may operate on either a single counter or any combination of counters simultaneously using a user-defined selection mask.

Command	Function
0	Clear one or more counters. If a counter is running at the time it is cleared, it will continue
1	Load counter with user-defined 32-bit value
2	Select count direction, up or down
4	Enable / disable counting
5	Latch counter; a counter must be latched before its count value can be read back. The latch is a snapshot of the counter value at one moment in time. The counter continues to run after latching.
6	Select clock source for one or more counters. Options include internal 50MHz clock, internal 10MHz clock, or the counter's designated I/O pin on port C.
7	Enable / disable auto-reload
8	Enable counter output pulse on designated I/O pin on port C
9	Configure counter output pulse width; options include 1, 10, 100, or 1000 clock periods
10	Read counter value. A counter must be latched with command 5 before its contents can be read back.
15	Reset one more counters. When a counter is reset its configuration and contents are lost.

14.5.3 Counter I/O Signals

Counter clock and output signals may be made available on digital I/O port C pins as defined below. A counter can use its port C pin for either an external clock or its output signal, not both at the same time.

NOTE: The voltage levels of the counter I/O signals will match the configuration of the digital I/O circuit, either 3.3v or 5V depending on the DIO configuration jumper settings on jumper block JP1.

DIO pin	Input	Output
C0	Counter 0 clock	Counter 0 output
C1	Counter 1 clock	Counter 1 output
C2	Counter 2 clock	Counter 2 output
C3	Counter 3 clock	Counter 3 output
C4	Counter 4 clock	Counter 4 output
C5	Counter 5 clock	Counter 5 output
C6	Counter 6 clock	Counter 6 output
C7	Counter 7 clock	Counter 7 output

14.5.4 Counter Advanced Features

The DAQ circuit uses counter/timers to control the A/D sample rate for high speed sampling as well as the D/A waveform generator data rate. These operations are managed by the Universal Driver software. Refer to the Universal Driver user manual for details on these advanced features.

14.6 Pulse Width Modulator Features

14.6.1 Overview

Zeta "A" models include 4 24-bit pulse width modulator circuits (PWMs). These circuits can be programmed to produce an output square wave up to 25MHz with a duty cycle anywhere from 0% to 100% (these limits are of course DC signals). The output polarity is programmable. PWM outputs are available on digital I/O port C pins.

PWM operation is as follows: Each PWM contains a period counter and a duty cycle counter which are programmed for the desired values. When the PWM starts, both counters start to count down simultaneously, and the output pulse is set to the desired active polarity. When the duty cycle counter reaches 0, it stops, and the output changes to the inactive polarity. When the period counter reaches zero, both counters reload, the output is made active again, and the cycle repeats.

The PWM duty cycle can be updated in real time without having to stop the circuit from running.

14.6.2 PWM Commands

The PWMs are configured and managed with a series of commands. These commands are implemented in the Diamond Systems Universal Driver software. Configuration commands operate on a single PWM at a time, however start, stop, and reset commands may operate on a single PWM or all PWMs at the same time.

Command	Function
0	Stop one or all PWMs. When a PWM is stopped, its output returns to its inactive state, and the counters are reloaded with their initial values. If the PWM is subsequently restarted, it will start at the beginning of its waveform, i.e. the start of the active output pulse. Stopping a PWM is not the same as resetting it. See command 4 below.
1	Load the period or duty cycle counter with user-defined value
2	Select output pulse polarity
3	Enable / disable PWM output. This must be done in conjunction with command 5 below.
4	Reset one or all PWMs. When a PWM is reset, it stops running, and any DIO line assigned to that PWM for output is released to normal DIO operation. The direction of the DIO line will revert to its value prior to the PWM operation.
5	Enable / disable PWM output signal on designated Port C DIO pin.
6	Select clock source for period and duty cycle counters, either 50MHz or 1MHz. Both counters will use the same clock source.
7	Start one or all PWMs. All selected PWMs will start their active output pulses at the same time.

14.6.3 PWM Output Signals

When a PWM output is enabled with command 5, the corresponding DIO pin on port C is forced to output mode regardless of its current configuration. To make the pulse appear on the output pin, command 3 must also be executed, otherwise the output will be held in inactive mode (the opposite of the selected polarity for the PWM output). When a PWM is reset, the corresponding digital I/O line returns to its previous direction and data status. PWM signals are available on digital I/O port C pins as defined below.

NOTE: The voltage levels of the PWM signals will match the configuration of the digital I/O circuit, either 3.3v or 5V depending on the DIO configuration jumper settings on jumper block JP1.

DIO Bit	*Alternate Signal*
C4	PWM 0 output
C5	PWM 1 output
C6	PWM 2 output
C7	PWM 3 output

14.7 Interrupt Operation

14.7.1 Overview

Interrupts provide a means for a circuit to request service from the processor autonomously without requiring the application software to continuously poll the circuit. When the circuit requires attention, it generates an interrupt request signal to the processor. The processor responds by passing program control to a dedicated software routine, which provides the functionality required by the circuit.

The maximum interrupt rate is not a fixed value but varies with the operating system and the duration that the interrupt service routine runs. The maximum rate must be determined by trial and error. However, a general guideline is that for Linux and Windows the rate should not exceed 1KHz. Because all interrupts require some processing overhead, the lower the rate the better. However, in the case of A/D sampling, a slower interrupt rate also delays the availability of new data. The programmer must find the ideal balance between processor load and response time.

The primary host interface for the Zeta base board "A" model data acquisition circuit is the SPI bus. However, the SPI bus does not provide a means to support interrupt operation. Therefore, Zeta base board "A" models provide the ability to generate interrupts on the ISA bus.

The ISA interrupt level, or IRQ number, can be chosen from among IRQ 5 and 7. The chosen interrupt level is dedicated to the data acquisition circuit and cannot be shared with other add-on PC/104 boards. The Zeta board BIOS provides support for up to 4 other IRQs for PC/104 boards. These IRQs are configured in the BIOS setup screens.

14.7.2 Interrupt Sources

Interrupts can come from several sources in the data acquisition circuit. A status register is used to indicate which circuit or circuits are requesting interrupt service, so the application software can respond accordingly.

A/D converter: For high speed sampling, the data acquisition circuit supports the use of interrupts to pass data back to the processor in large blocks instead of one sample at a time. This greatly reduces the processor time required to handle the data flow. A programmable FIFO holds the A/D data and generates an interrupt request when the number of samples in the FIFO reaches a user-specified threshold. This is described more fully in the data acquisition section above.

Counter/timers: Counters 2 and 3 can be used to generate interrupts at programmable frequencies. Generally, only one or the other counter is used for interrupts, however it is possible to use both simultaneously.

Edge detection circuit: As described above, digital I/O port B can be used to monitor the state of up to 8 digital inputs and generate an interrupt request when a specific transition is seen on any of its 8 inputs.

15 “D” Model Digital I/O

Zeta “D” models provide 16 digital I/O coming from an I2C I/O expander chip. The digital I/O consists of 16 I/O lines organized as two 8-bit ports A and B. They may be configured with a jumper for either 3.3V or 5V logic levels, and they may also be configured with a jumper for 10K ohm pullup or pull-down resistors. These jumper settings apply to both ports collectively; it is not possible to configure one port for 3.3V and the other for 5V at the same time, or to configure one port for pull-up and other for pull-down simultaneously. For safety and to prevent glitches, on power up or reset, all ports reset to input mode and all port data registers reset to all 0.

Source code and detailed instructions for “D” model DIO features are downloadable from the Diamond Systems website www.diamondsystems.com.

- 16 digital I/O lines
- Programmable direction in 8-bit groups
- User-selectable 3.3V / 5V logic levels
- User-selectable 10K pull-up / pull-down resistors

The circuit controller is PCA9535 I2C to GPIO Expander that interfaces to the processor via the I2C bus from COM express connector. 7bit I2C address for the GPIO expander is 0x22. Please refer Section Digital I/O (J15) Digital IO Connector pinouts.

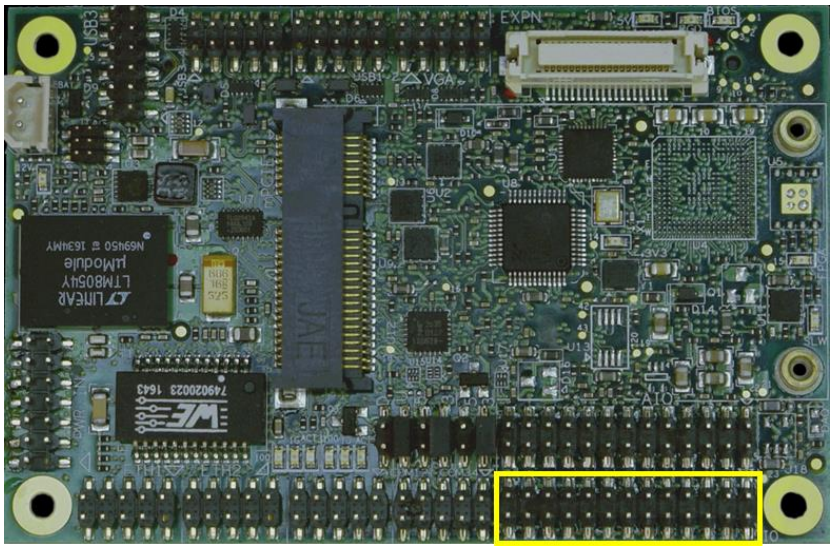


Figure 13: Digital I/O connector

15.1 Block Diagram

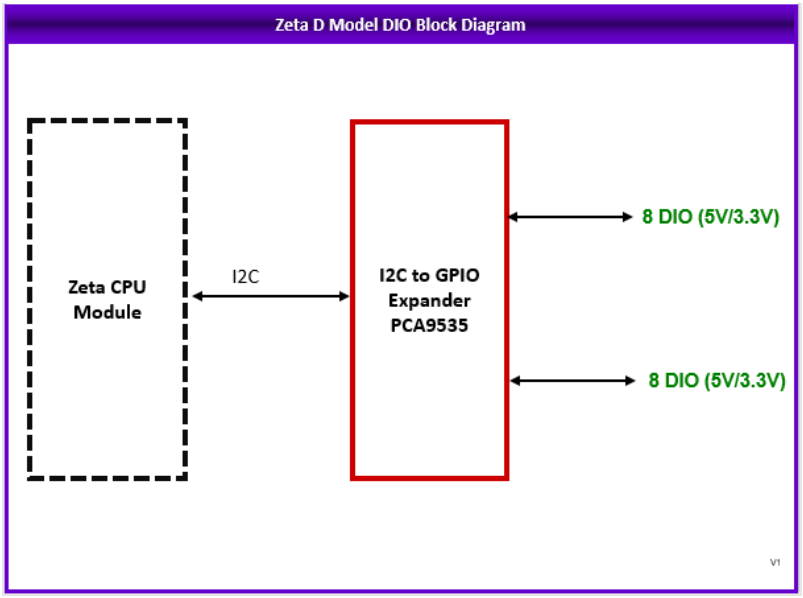


Figure 14: D Model Digital I/O Block Diagram

15.2 Digital IO specification

No of IO lines	16
Direction	Programmable bit by bit.
Polarity	Programmable bit by bit
Input voltage	VDD= 5V
Logic 0:	0.0V min, 1.5V max, ±1uA
Logic 1:	3.5V min, 5.5V max, ±1uA
Output Voltage	VDD= 5V
Logic 0:	0.0V min, 0.7V max, +14mA(Typ)
Logic 1:	4.1V min, 5.0V max, -10mA(Typ)
Input voltage	VDD= 3.3V
Logic 0:	0.0V min, 0.99V max, ±1uA
Logic 1:	2.31V min, 3.3V max, ±1uA
Output Voltage	VDD= 3.3V
Logic 0:	0.0V min, 0.7V max, +14mA(Typ)
Logic 1:	2.65V min, 3.3V max, -10mA(Typ)

15.3 Configuration and Programming

Please refer the PCA9535 Datasheet (available via online search) for programming instructions for the digital I/O. The PCA9535 uses I2C address 0100 010x (where x is the read/write- bit). The PCA9535 has 4 registers for each 8-bit data register: An input register, an output register, a polarity register, and a direction register. DIO port A (J15 pins 1-8) corresponds to PCA9535 port 0, and DIO port B (J15 pins 9-16) corresponds to PCA9535 port 1.